LED171596A 96-LED Matrix Driver for RGB and White LEDs

1 Features

- 24 High-Precision Current Sinks
  - 60-mA Peak Current per Channel
  - Current Matching ±5%
  - Independent 9-Bit Duty Cycle PWM and 8-Bit LED Current Control
  - 7-V Tolerant
  - ISET Resistor to Set Global Current
  - Ghosting Cancellation
- Four Low Resistance High Side Series Switches
  - 1.5-A Current-Rated PMOS
- I^2C, SPI, and PWM Brightness Control Modes
- Extensive Protection Features
  - Open and Shorted LED Fault Detection
  - Thermal Shutdown Protection

2 Applications

- Control Panel Illumination
- Local Dimming LED Backlight Drivers

3 Description

The LED171596A is a 96 channel matrix LED driver with independent channel control, designed for driving locally dimmed displays. The device sports 4 low-resistance high side switches and 24 low side current sinks that can deliver up to 15 mA of continuous current per channel. The driver has 9-bit duty cycle and 8-bit current control of each low-side LED current sink.

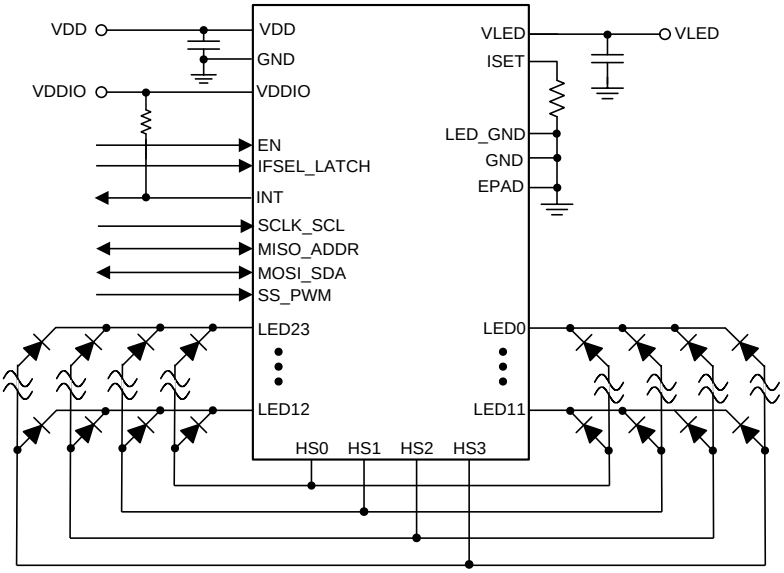
Each current sink can be individually controlled through the I^2C-compatible or SPI interface, but also has the capability to be controlled with a single value through the global brightness control register. This global brightness control also passes through a brightness sloper function to create optically smooth brightness transitions without the need for multiple register writes.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LED171596A	VQFN (48)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2017) to Revision A	Page
• First release of production-data data sheet	1

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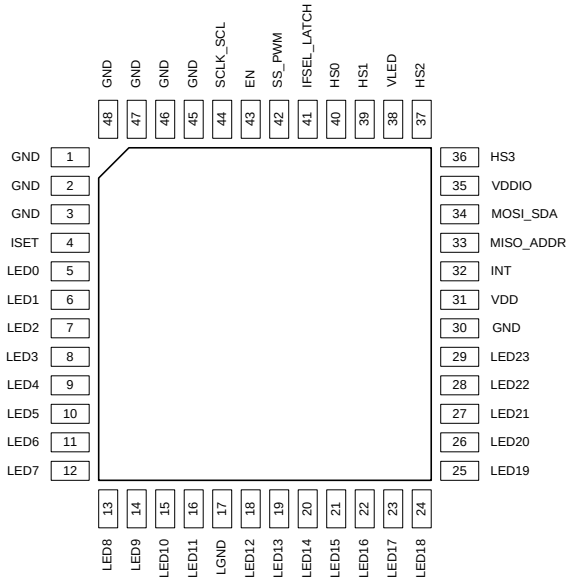
5 Pin Configuration and Functions

RSL Package
48-Pin VQFN With Thermal Pad
Top View



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Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	GND	Ground	Connect to Ground.
2	GND	Ground	Connect to Ground.
3	GND	Ground	Connect to Ground.
4	ISET	Analog	Connection for external resistor to globally set the maximum current for each current sink (RSET = 750/ILED_MAX)
5	LED0	Analog	Constant-current output
6	LED1	Analog	Constant-current output
7	LED2	Analog	Constant-current output
8	LED3	Analog	Constant-current output
9	LED4	Analog	Constant-current output
10	LED5	Analog	Constant-current output
11	LED6	Analog	Constant-current output
12	LED7	Analog	Constant-current output
13	LED8	Analog	Constant-current output
14	LED9	Analog	Constant-current output
15	LED10	Analog	Constant-current output
16	LED11	Analog	Constant-current output
17	LGND	Ground	LED-driver ground
18	LED12	Analog	Constant-current output
19	LED13	Analog	Constant-current output
20	LED14	Analog	Constant-current output
21	LED15	Analog	Constant-current output

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
22	LED16	Analog	Constant-current output
23	LED17	Analog	Constant-current output
24	LED18	Analog	Constant-current output
25	LED19	Analog	Constant-current output
26	LED20	Analog	Constant-current output
27	LED21	Analog	Constant-current output
28	LED22	Analog	Constant-current output
29	LED23	Analog	Constant-current output
30	GND	Ground	Ground for analog and digital circuitry
31	VDD	Power	3.3-V supply for analog and digital circuitry
32	INT	Output	Interrupt pin. Open drain output. Pull up to VDDIO
33	MISO_ADDR	Input / Output	SPI master in, slave out, and I^2C address select input
34	MOSI_SDA	Input / Output	SPI master out, slave in, and I^2C data. When configured for I^2C, pull up to VDDIO required.
35	VDDIO	Power	Reference and power supply for logic pins
36	HS3	Analog	High-side PMOS switch output for LED group 3
37	HS2	Analog	High-side PMOS switch output for LED group 2
38	VLED	Power	Input pin for high-side switches
39	HS1	Analog	High-side PMOS switch output for LED group 1
40	HS0	Analog	High-side PMOS switch output for LED group 0
41	IFSEL_LATCH	Input	IFSEL = 1 selects I^2C-compatible interface and IFSEL = 0 selects SPI interface after EN pin set high. Optional latch input for brightness and current register buffers when in normal mode.
42	SS_PWM	Input	SPI slave select and global PWM input
43	EN	Input	Enable (internally pulled low)
44	SCLK_SCL	Input	SPI serial clock and I^2C clock input. When configured for I^2C, pull up to VDDIO required.
45	GND	Ground	Connect to Ground
46	GND	Ground	Connect to Ground
47	GND	Ground	Connect to Ground
48	GND	Ground	Connect to Ground
	Exposed Thermal Pad		Must be connected to GND (pins 1, 2, 3, 30, 45, 46, 47 and 48), LGND (pin 17) and common ground plane. See the *Figure 312*. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage on pins	VLED, LED0…LED23	-0.3	7	V
	VDD, VDDIO, ISET	-0.3	3.6	
	EN, IFSEL_LATCH, SCLK_SCL, MISO_ADDR, MOSI_SDA, SS_PWM, INT	-0.3	VDDIO	
Thermal	Continuous power dissipation	Internally limited		
	Ambient temperature	–40	85	°C
	Junction temperature	–40	125	°C
	Maximum lead temperature (soldering)	SLMA002		°C
Storage temperature, T_{stg}		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	TYP	MAX	UNIT
Voltage on pins	VLED			6.1	V
	LED0…LED23			V_{LED}	V
	VDD Operating	2.9	3.3	3.5	V
	VDD Startup	3.0	3.3	3.5	V
	VDDIO	1.65	1.8/3.3	3.5	V
	EN, IFSEL_LATCH, SCLK_SCL, MISO_ADDR, MOSI_SDA, SS_PWM, INT			V_{DDIO}	V
Thermal	Ambient temperature	–40		85	°C

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (TA-MAX) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125ºC), the maximum power dissipation of the device in the application (PD-MAX), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$.

6.4 Thermal Information

THERMAL METRIC[1]		LED171596A RSL (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	5.1	
$\Psi_{\theta JT}$	Junction-to-top characterization parameter	0.2	
$\Psi_{\theta JB}$	Junction-to-board characterization parameter	5.0	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.2	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Limits apply over the full ambient temperature range –40°C > T_A > +85°C. Unless otherwise specified: V_{DD} = 3.3 V, V_{DDIO} = 3.3 V_{LED} = 5V, I_{LED_PK} = 60 mA, C_{VLED} = 10 µF, C_{VDD} = 1 µF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
V_{DD}	VDD supply votage	Startup	3.0	3.3	3.5	V
		Normal Operation	2.9	3.3	3.5	
V_{DD} I_Q	Shutdown mode current	EN = L,			15	uA
	Standby mode current	EN = H, LEDs drivers disabled		7	9	mA
	Normal mode current	EN = H, 20-mA peak per LED, 100% duty		37	60	mA
		EN = H, 60-mA peak per LED, 100% duty		99	160	
VDD_{POR}	VDD power-on reset threshold	V_{DD} rising, POR releases	2.81	2.88	2.95	V
		V_{DD} falling, POR activates	2.71	2.78	2.85	
T_{TSD}	Thermal shutdown threshold			150		°C
T_{TSD_THR}	Thermal shutdown hysteresis			20		°C
V_{DDIO}	VDDIO supply voltage		1.65	1.8/3.3	3.5	V
VDDIO I_Q	VDDIO supply current	Serial interface idle		2	5	uA
LED CURRENT SINK AND LED PWM						
$I_{LEAKAGE}$	Leakage current	LED0 to LED23, V_{LED} = 6.1 V			1	uA
I_{MAX}	LED sink current (peak)	LED0 to LED23, R_{ISET} = 12.5 kΩ	55.7	60	63.6	mA
$I_{ACCURACY}$ [1]	Output current accuracy	I_{OUT} = 60 mA, PWM duty =100%	-7		7	%
I_{MATCH} [2]	Output current matching	I_{OUT} = 60 mA, PWM duty =100%	-5		5	%
V_{SAT} [3]	Saturation voltage	I_{OUT} = 60 mA	215	405	600	V
		I_{OUT} = 20 mA	50	153	255	
$OUTPWM_{RES}$	LED PWM resolution			9		bit
t_{RISE}	LED output rise time	I_{OUT} = 60 mA		30		ns
$V_{LEDOPEN}$	LED open detection threshold	drv_headroom[1:0] = 00b	0.075	0.27	0.5	V
		drv_headroom[1:0] = 01b	0.36	V_{SAT}+0.25	0.97	
		drv_headroom[1:0] = 10b	0.6	V_{SAT}+0.5	1.22	
		drv_headroom[1:0] = 11b	0.85	V_{SAT}+0.75	1.5	

(1) Output Current Accuracy is the difference between the actual value of the output current and programmed value of this current.
(2) Matching is the maximum difference from the average. For the constant current outputs on the part (LED0 to LED23), the following are determined: the maximum output current (MAX), the minimum output current (MIN), and the average output current of all outputs (AVG). Two matching numbers are calculated: (MAX-AVG)/AVG and (AVG-MIN)/AVG. The largest number of the two (worst case) is considered the matching figure.
(3) Saturation voltage is defined as the voltage when the LED current has dropped 10% from the value measured at 1V.

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Electrical Characteristics (continued)

Limits apply over the full ambient temperature range –40°C > T_A > +85°C. Unless otherwise specified: V_{DD} = 3.3 V, V_{DDIO} = 3.3 V_{LED} = 5V, I_{LED_PK} = 60 mA, C_{VLED} = 10 µF, C_{VDD} = 1 µF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{LEDSHORT}$	LED short detection threshold	V_{LED} = 5V	3.7	4	4.3	V
HIGH SIDE SWITCH						
V_{LED} I_Q	V_{LED} Leakage	V_{DD} = 0V, EN = L			3	uA
	Shutdown mode current	V_{LED} = 6.1V, EN = L	6.8	14.8	28.7	uA
	Normal mode current	V_{LED} = 6.1V, EN = H, ENABLES = 0x01, LED_DRIVER_CONTROL =0x0	115	182	225	uA
R_{DSON}	High-side PMOS ON-resistance	V_{LED} ≥ 4V	80	160	330	mΩ
		1.914 ≤ V_{LED} ≤ 6.034	80	356	650	mΩ
LOGIC INPUT EN						
V_{IL}	Input low level	V_{DDIO} = 1.8			0.2 × VDDIO	V
V_{IH}	Input high level	V_{DDIO} = 1.8	0.8 × VDDIO			V
I_I	Input current	V_{PIN} ≤ V_{DDIO}	0.7	3.6	6.5	uA
R_{PD}	Input resistor		0.6	1	4.7	MΩ
LOGIC INPUT IFSEL_LATCH, SCLK_SCL, MOSI_SDA, MISO_ADDR, SS_PWM						
V_{IL}	Input low level	VDDIO = 1.8			0.2 × VDDIO	V
V_{IH}	Input high level	VDDIO = 1.8	0.8 × VDDIO			V
I_I	Input current	V_{PIN} ≤ V_{DDIO}	−1		1	uA
LOGIC INPUT PWM						
f_{PWM_IN}	PWM input frequency		0.1		20	kHz
$t_{ON_OFF_MIN}$	PWM input minimum on/off time		200			ns
$INPWM_{RES}$	PWM input resolution			9		bits
LOGIC OUTPUT INT						
$VINT_{OL}$	Output low level	I_{OUT} = 3 mA		0.3	0.5	V
$IINT_{LEAK}$	Output leakage current				1	uA
LOGIC OUTPUT MISO						
$VSDO_{OL}$	Output low level	I_{OUT} = 3 mA		0.3	0.5	V
$VSDO_{OH}$	Output high level	I_{OUT} = –2 mA	0.7 × VDDIO	0.9 × VDDIO		V
$ISDO_{LEAK}$	Output leakage current	V_{PIN} ≤ V_{DDIO}			1	uA
LOGIC OUTPUT SDA						
$VSDA_{OL}$	Output low level	I_{OUT} = 3 mA		0.3	0.5	V
$ISDA_{LEAKAGE}$	Output leakage current	V_{SDA} = V_{DDIO} =3.5 V			1	uA

6.6 Timing Requirements for EN, IFSEL_LATCH

		MIN	TYP	MAX	UNIT
t_{EN}	Time from EN rising edge until SPI or I^2C first access			5	ms
$t_{DISABLE}$	EN low time for reset detection			0.125	ms
t_{IFSEL_HOLD}	IFSEL_LATCH hold time following EN rising edge			1	ms
t_{LATCH}	Minimum LATCH pulse width	500			ns

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6.7 Timing Requirements for SPI Interface

		MIN	TYP	MAX	UNIT
t1	Cycle time	100			ns
t2	Enable lead time	50			ns
t3	Enable lag time	50			ns
t4	Clock low time	45			ns
t5	Clock high time	45			ns
t6	Data setup time	20			ns
t7	Data hold time	20			ns
t8	Disable time			30	ns
t9	Data valid			35	ns
t10	SS inactive time	50			ns
Cb	Bus capacitance	5		40	pF

6.8 Timing Requirements for I²C Interface

		MIN	TYP	MAX	UNIT
fscl	Clock frequency			1	MHz
1	Hold time (repeated) START condition	260			ns
2	Clock low time	500			ns
3	Clock high time	260			ns
4	Set-up time for repeated START condition	260			ns
5	Data hold time	0			ns
6	Data set-up time	50			ns
7	Rise time of SDA and SCL			120	ns
8	Fall time of SDA and SCL			120	ns
9	Set-up time for STOP condition	260			ns
10	Bus free time between a STOP and START condition	500			ns
11	Data valid acknowledge time	50		450	ns
12	Data valid time	50		450	ns

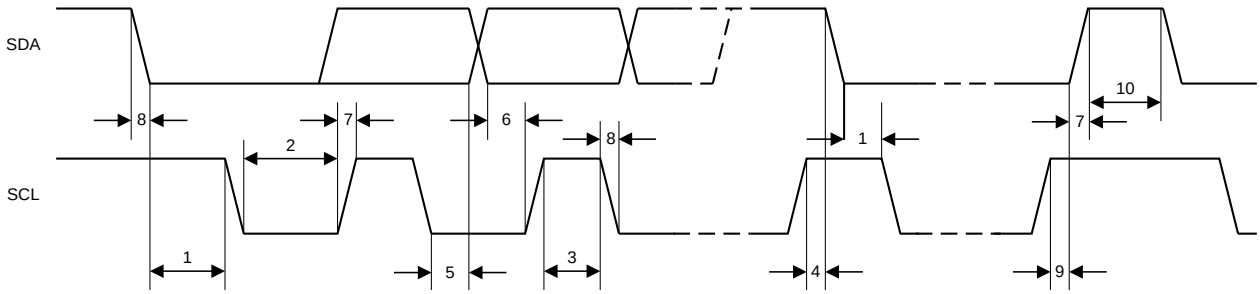

Figure 1. I²C Timing

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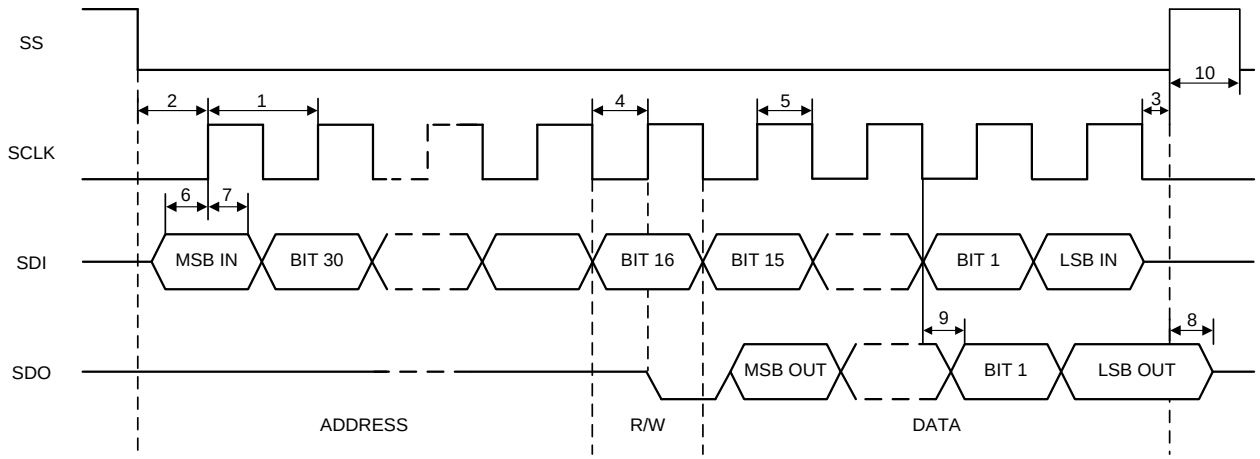


Figure 2. SPI Timing

6.9 Typical Characteristics

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–40°C < T_A < +85°C), V_{DD} = 3.3 V, V_{DDIO} = 3.3 V_{LED} = 5 V, I_{LED_PK} = 60 mA, C_{VLED} = 10 µF, C_{VDD} = 1 µF,

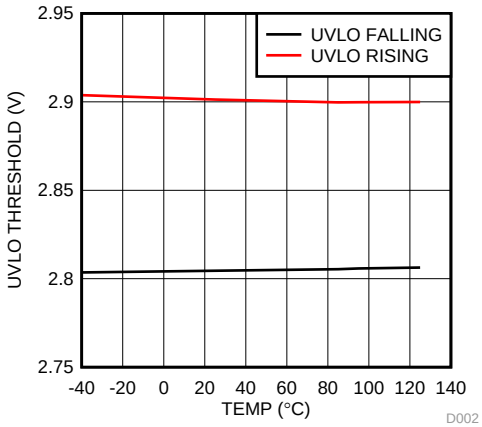


Figure 3. VDD UVLO Rising and Falling Thresholds

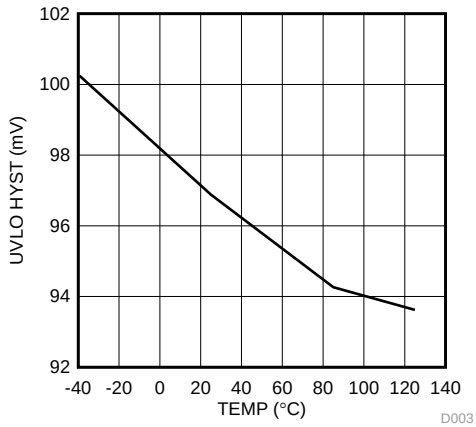
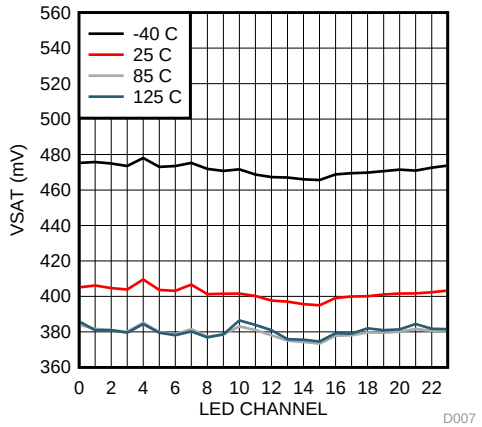
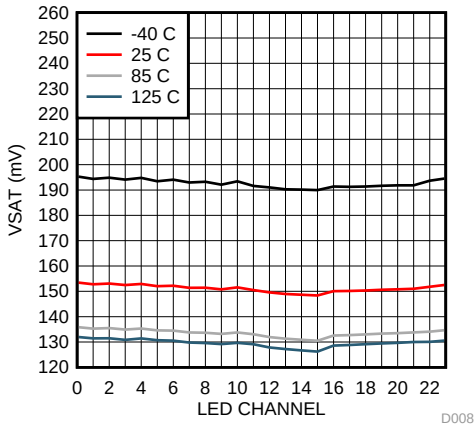


Figure 4. VDD UVLO Hysteresis



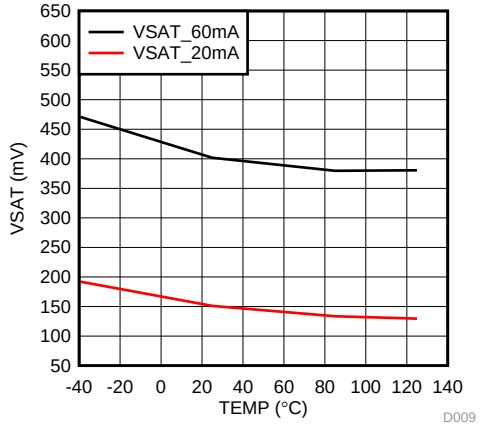
ISET = 12.5 kΩ

Figure 5. VSAT vs LED Channel



ISET = 37.5 kΩ

Figure 6. VSAT vs LED Channel



ISET = 12.5 kΩ and 37.5 kΩ

Figure 7. VSAT vs Temperature

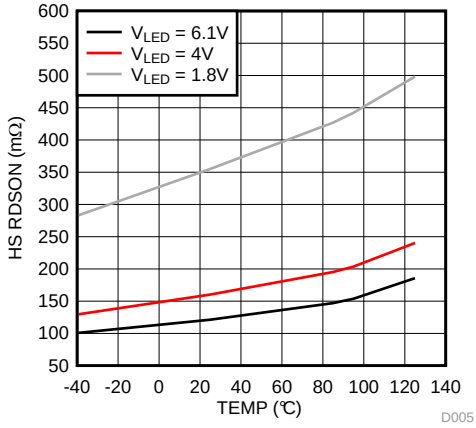


Figure 8. High Side Switch R_{DSON}

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Typical Characteristics (continued)

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–40°C < T_A < +85°C), V_{DD} = 3.3 V, V_{DDIO} = 3.3 V_{LED} = 5 V, I_{LED_PK} = 60 mA, C_{VLED} = 10 µF, C_{VDD} = 1 µF,

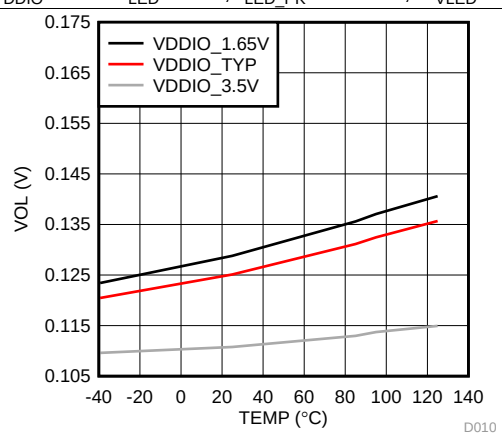

Figure 9. VOL vs Temperature

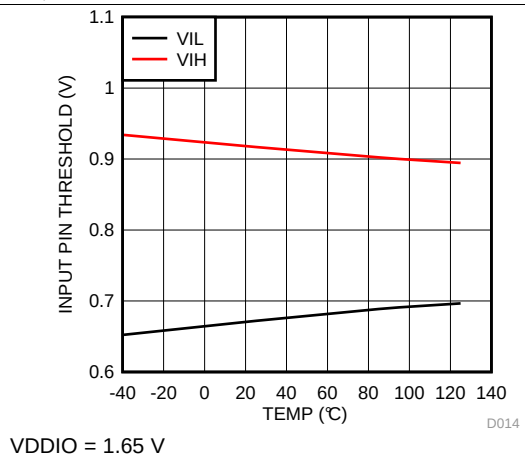

Figure 10. VIH and VIL vs Temperature

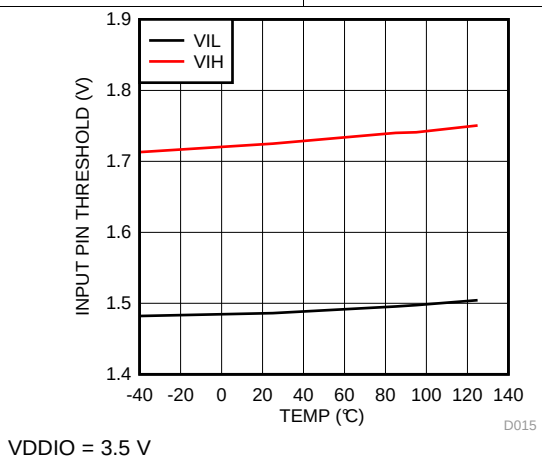

Figure 11. VIH and VIL vs Temperature

7 Detailed Description

7.1 Overview

The LED171596A is a LED driver that can individually control up to 96 LEDs. To control the 96 LEDs in a 4 × 24 matrix the device uses four high-side PMOS switches and 24 low-side programmable current sinks. Each of the low-side current sinks has independent 9-bit duty cycle and 8-bit current control. The individually duty and current values can be controlled through the SPI or I^2C-compatible interfaces.

The four high-side switches allow the LED171596A to time multiplex four groups of 24 LEDs. Maximum peak current is set with ISET (with 60 mA maximum), but the maximum average current delivered to each LED is 15 mA (ILED_MAX /4).

The individual LED brightness is internally multiplied with a global brightness register value. This allows the control of all the LEDs at once with a single master brightness register or PWM input signal. This master brightness also passes through a brightness sloper function to create optically smooth brightness transitions without the need for multiple register writes.

Device control interface features:

- EN is an enable input for LED171596A
- INT is an open-drain interrupt output (indicating fault condition detection or sloper completion, for example)
- IFSEL_LATCH is a dual function pin which is used for selecting between I^2C-compatible and SPI after rising edge of EN pin then can be used to latch register changes.
-
  - For interface selection the IFSEL pin status is checked after rising edge of EN pin. Note: IFSEL must be static for t_{IFSEL_HOLD} max time following EN rising edge.
    - If IFSEL is pulled low (0) the 4-wire SPI interface is selected (SCLK, MISO, MOSI, and SS).
    - If IFSEL is pulled high (1) the 2-wire I^2C-compatible interface is selected.
      - An optional PWM input is available at SS/PWM when I^2C is selected.
      - When I^2C is selected, the ADDR pin is used to select between three alternate I^2C slave addresses.
  - In normal mode the pin functions as a LATCH signal to trigger updates of SRAM buffers.
    - LATCH occurs on the rising edge. Minimum latch pulse length is t_{LATCH} ns.
    - Alternatively a LATCH register bit can be used instead of pin control. Wait for latch_busy to be cleared in STATUS register before writing to SRAM when using LATCH register bit.
- ISET pin to set master LED current level for all LEDs.

Protection features of the LED171596A device include:

- Open-LED and shorted-LED detections
  - When detected (unless masked), the INT pin goes low, and status registers show that LEDs are OPEN or SHORT. Faulty LEDs can then be disabled via register bits, and fault status can be cleared.
- Thermal shutdown in case of die overtemperature

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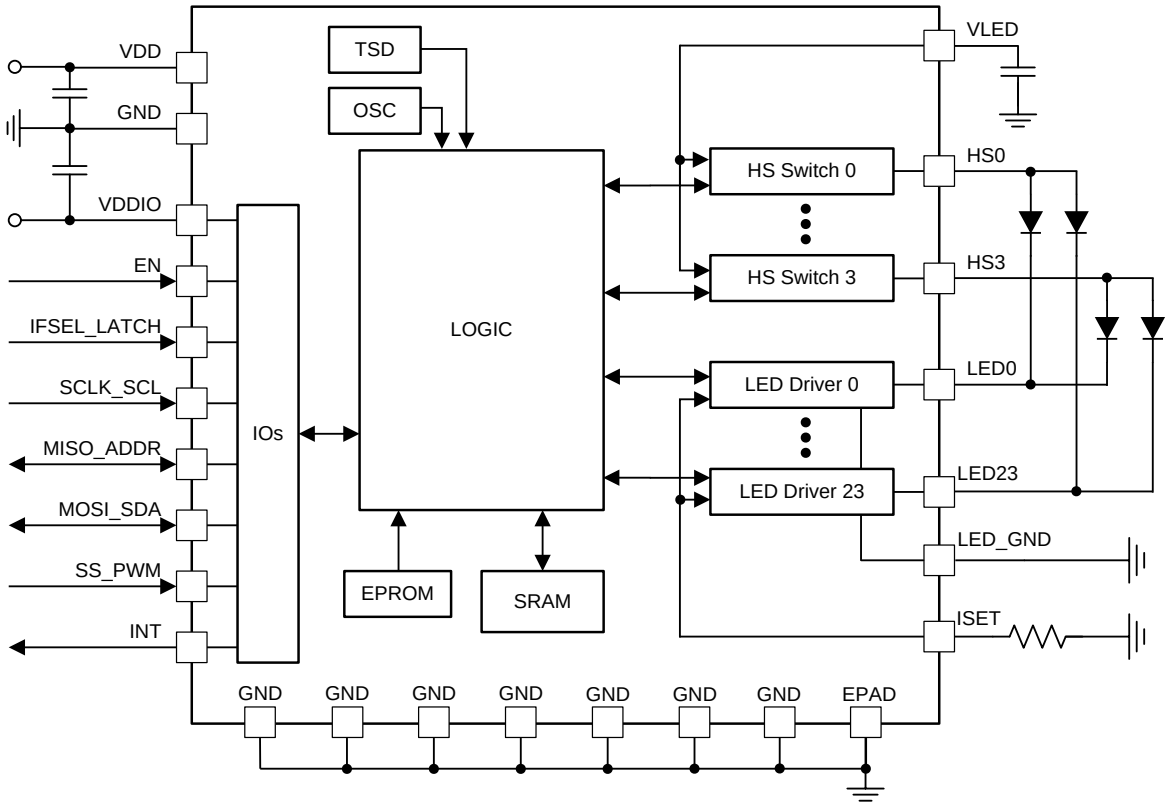
7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Control Interface

Register control interface is selected with IFSEL pin according to Table 1.

Table 1. Serial Control Interface Selection

IFSEL PIN	SERIAL INTERFACE
VDDIO (1)	I^2C-compatible
GND (0)	SPI

The SPI interface of the LED171596A device supports up to 10 MHz using a 16-bit register addressing. In I^2C mode it supports up to 1-MHz fast-mode-plus specification. The I^2C and SPI interfaces are available to use after t_{EN} , following the rising edge of the EN pin. Following start-up and IFSEL detection (t_{IFSEL_HOLD} max), the LATCH pin functionality is enabled to start SRAM buffer updates. The LATCH pulse duration must be at least t_{LATCH} ns. Alternatively, the LATCH register bit can also be used.

7.3.2 Matrix Control Scheme

The LED171596A utilizes four LED phases to multiplex the 24 LED current sinks providing control of up to 96 LEDs. Four cathodes can be connected to each LEDx pin and each of their anodes are connected to HS0 thru HS3. Brightness (Duty) and Current registers are programmable for each LED. The sequencer automatically selects the correct brightness and current values as it cycled through each of the four LED matrix phases (see Figure 12).

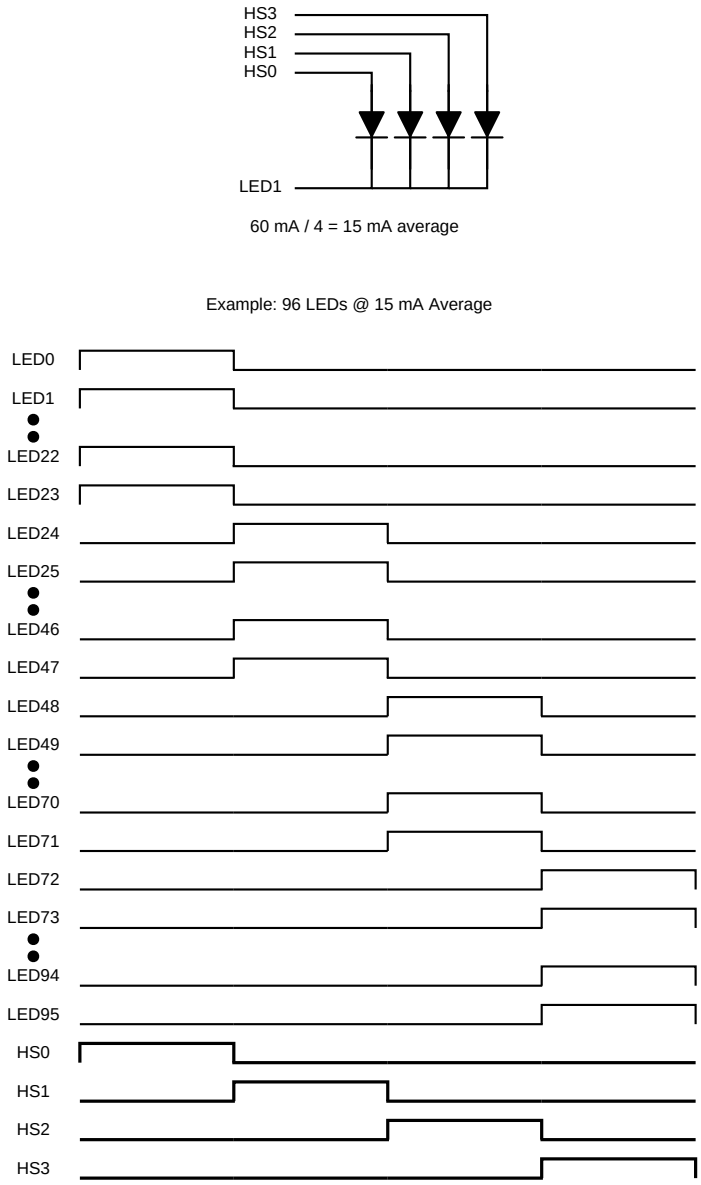

Figure 12. LED171596 4 × 24 Matrix Sequence (Ghosting Cancellation Disabled)

7.3.3 LED Current Sinks

7.3.3.1 LED Output Current Setting

The RISET resistor is used to set the maximum LED current for all LED driver outputs. The LEDXX_CUR[7:0] registers are used to individually adjust the current of each from zero to the maximum. Equation 1 is used to calculate the current setting of an individual LED in this mode.

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$$I_{LED(XX)} = \frac{750}{R_{ISET}} \times \frac{ledxx_cur[7:0]}{255} \quad (1)$$

For example, a 12.5-kΩ RISET results in a 60-mA maximum peak current. Each LEDXX_CUR LSB adjusts the individual LED current by 235–µA steps. Smaller individual current adjustment steps are achieved when using a lower maximum peak current (larger RISET value). For example, a 25-kΩ RISET results in a 30-mA maximum peak current and 118-µA steps per LEDXX_CUR LSB.

7.3.3.2 LED PWM Frequency

The LED171596A supports 10-kHz or 20-kHz pwm output frequency. The pwm frequency is configured using the CONFIG_PWM register bit [4]. An internal 40-MHz oscillator is used for generating PWM outputs. When CONFIG_PWM register bit 4 is high the reference clock is divided by 2.

7.3.3.3 LED Driver Group Turnon Delay

The 24 LED current sinks turn on in four different groups with a programmable delay between groups. The delay is configured using the PWM_PHASE_SHIFT_CONFIG register bits [1:0] to select from 0, 1, 2, or 3 reference clock delays. This delay reduces inrush currents and reduces maximum LED on-time. The first group consists of LED0, 4, 8, 12, 16, and 20 which turn on with no delay and turn off up to 3 clocks before the maximum on-time. The second group consists of LED1, 5, 9, 13, 17 and 21, which turn on and off up to 3 clocks after the first group. The third group consists of LED2, 6, 10, 14, 18 and 22, which turn on and off up to 3 clocks after the second group. The fourth group consists of LED3, 7, 11, 15, 19, and 23, which turn on and off up to 3 clocks after the third group.

7.3.4 Brightness Control

The LED171596A supports individual brightness control for each LED through individual PWM duty cycle control of LED0...LED95 via I^2C/SPI registers. A master brightness register or PWM input is multiplied with each individual (LEDXX_BRI[8:0]) brightness register to allow control of every LED at once.

7.3.4.1 Brightness Control Signal Path

There are several methods to control the brightness level of each LED:

7.3.4.1.1 Master Brightness Control Method

Using master brightness control through master_bri register or PWM input (selectable by register bit enable_pwm_detector – PWM input is available only in I^2C mode). Master brightness control affects all LEDs simultaneously. Master brightness can change the LED brightness immediately or smoothly using the optional sloper block. Master brightness change requires a single write transaction so bus traffic is very low. A LATCH command is required if Master Brightness is controlled by register write (master_bri). The PWM input control can change the master brightness immediately without need of a LATCH command.

The individual LED PWM duty cycle is calculated using Equation 2 and Equation 3:

When enable_pwm_detector = 0:

$$\text{LEDxx PWM Brightness} = ledxx_bri \times master_bri \quad (2)$$

When enable_pwm_detector = 1:

$$\text{LEDxx PWM Brightness} = ledxx_bri \times \text{PWM input duty cycle} \quad (3)$$

NOTE

If master sloper is enabled then actual brightness value is sloping towards new master brightness value and thus takes time to reach the calculated value.

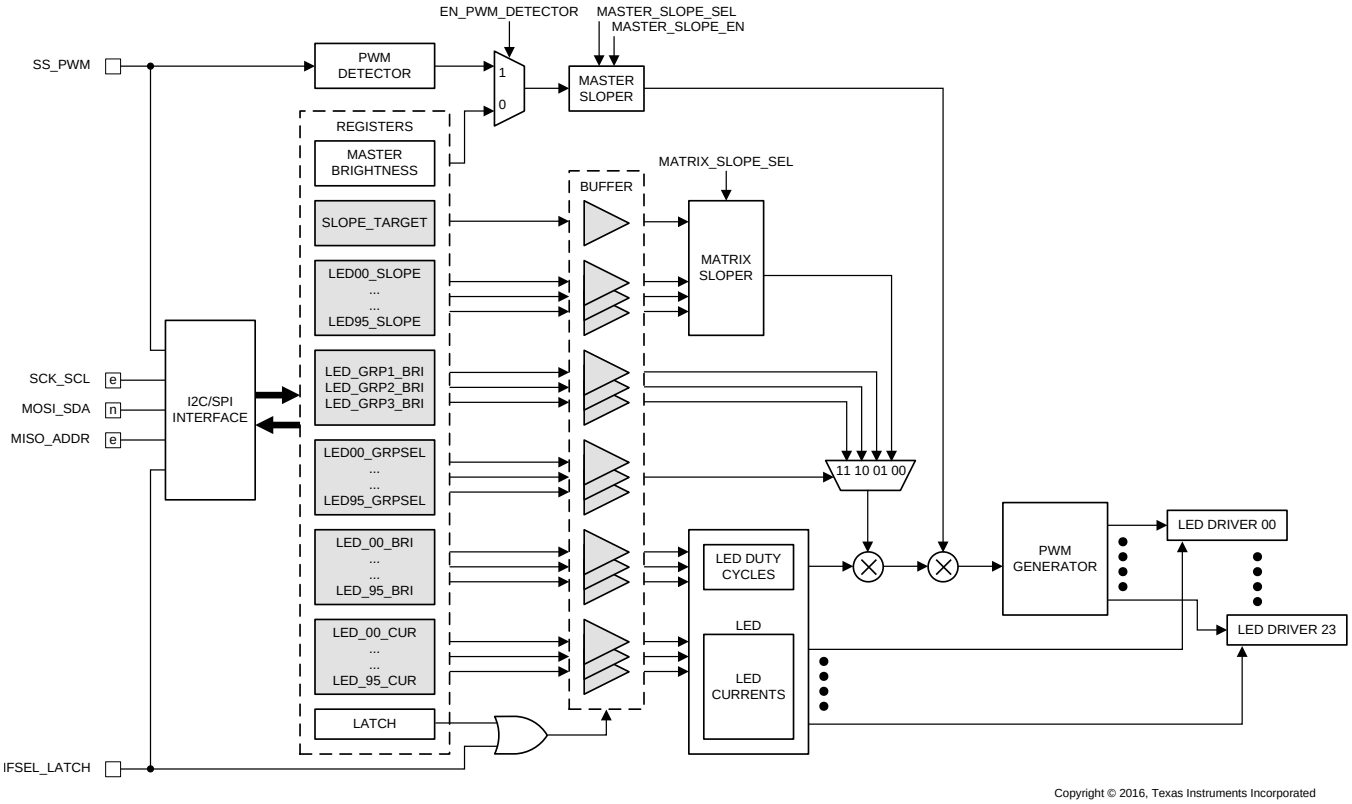

Figure 13. Brightness Path

7.3.4.1.2 Individual LED Brightness Control Method

Every LED has an individual brightness and current register that are used to change the LED brightness. The brightness and current registers of each LED are individually addressable, so if only one LED brightness must be changed then only one 9-bit register needs to be written. This reduces interface bus traffic compared to other devices. If all LEDs must be updated then up to 96 × 9-bit brightness, and 96 × 8-bit current registers must be written. A LATCH command is required to apply updated values.

7.3.4.1.3 Matrix Sloper Brightness Control Method

The matrix sloper block is used to control both up and down dimming for selected LEDs. LEDs are assigned to the matrix sloper using their individual LEDXX_SLOPE bits. There are 4 states of how the sloper control affects the selected LEDs:

1. LED or group of LEDs is not selected for dimming (brightness = 100%)
2. LED or group of LEDs is sloping toward target brightness value (100% → SLOPE_TARGET)
3. LED or group of LEDs is sloping toward 100% brightness value (SLOPE_TARGET → 100%)
4. LED or group of LEDs is kept at target value (SLOPE_TARGET)

The matrix sloper configuration starts by writing to the LEDxx_SLOPE registers (12 registers) for each LED. Selected LEDs must all be starting from the same LEDxx_BRI value. SLOPE_TARGET value and sloper duration registers are then configured. The LATCH signal (minimum t_{LATCH}) or register bit triggers the start of sloping. The INT signal is asserted when matrix sloper is done.

A special case is if one group of LEDs is dimming towards SLOPE_TARGET and the second group is dimming toward 100% at the same time.

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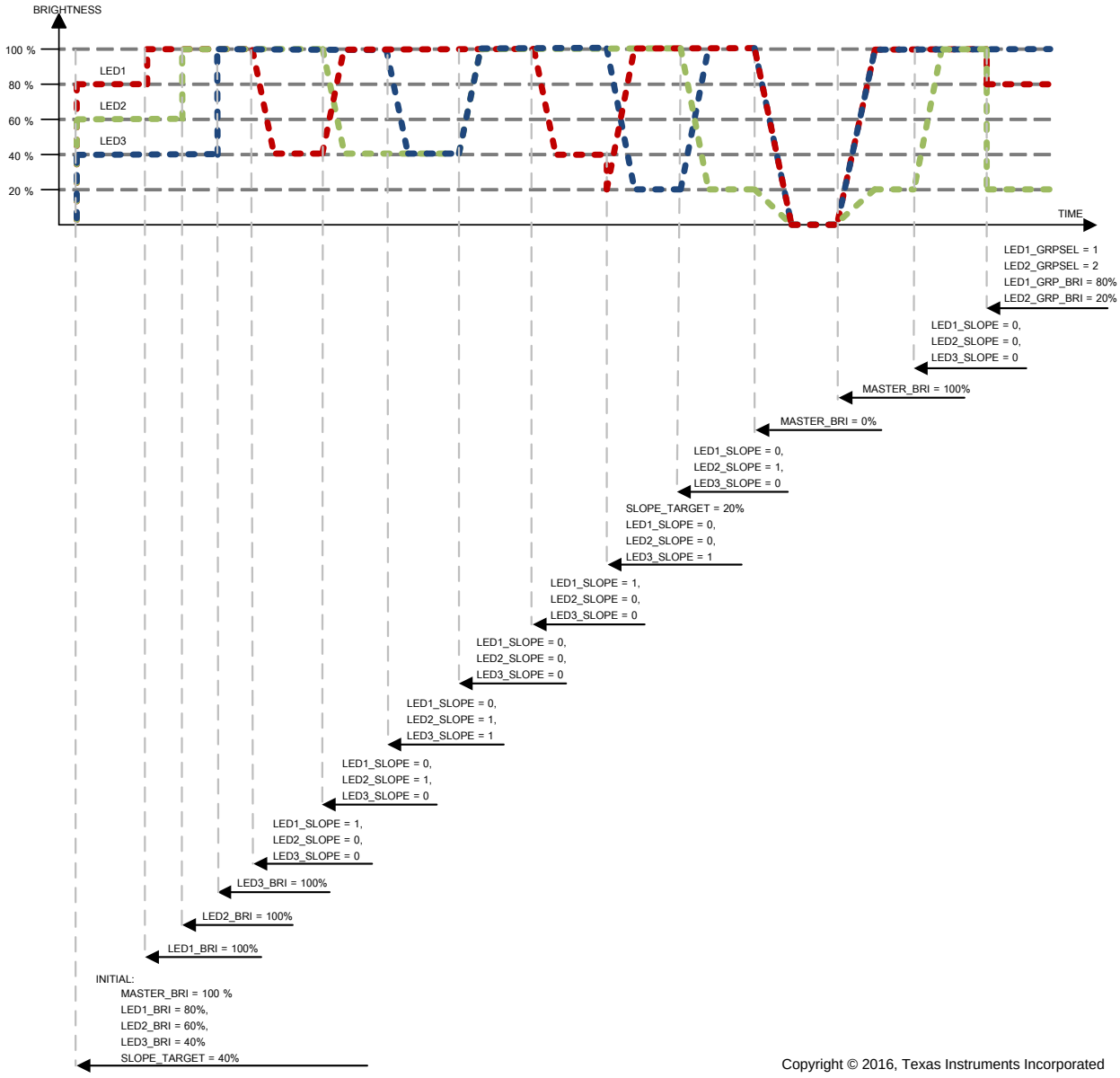

Figure 14. Sloper Function

Figure 14 shows examples of how the matrix sloper is used to slope the brightness of LEDs 1, 2, and 3. Each arrow represents brightness or configuration changes and a corresponding LATCH event. Figure 14 shows how the matrix sloper function affects LED output brightness when the corresponding LEDX_SLOPE bit is set.

7.3.4.1.4 Group Brightness Control Method

The group brightness control is used to select LEDs into 1 to 3 groups where each group has a separate register for brightness control. Every LED has 2-bit selection register LEDxx_GRPSEL to select whether or not it belongs to one of the three groups:

- 00 – Not a member of any group
- 01 – Member of group 1
- 10 – Member of group 2
- 11 – Member of group 3

The brightness level for each group is controllable with the LED_GRP1_BRI, LED_GRP2_BRI and LED_GRP3_BRI registers. The matrix sloper does not affect any LEDs that are assigned to these three groups. The master brightness register (MASTER_BRI) affects all LEDs regardless of group selection as shown in Equation 4.

$$\text{LEDxx PWM Brightness} = \text{ledgrp[1...3]_bri} \times \text{ledxx_bri} \times \text{master_bri} \tag{4}$$

7.3.4.2 Matrix Ghosting Cancellation

To avoid unwanted illumination (ghosting) of the LEDs not currently being driven, the LED171596A has an integrated ghosting cancellation function. The ghosting cancellation is performed in between the LED driving phases when the high side switches are transitioned. During this time the LED is reverse biased to discharge parasitic capacitances in the system (see Figure 15). Make sure your LED reverse breakdown voltage is higher than the VLED voltage being used in the system. Setting the hs_en_ghost_cancel and drv_en_ghost_cancel register bits to zero disables the LED ghosting cancellation function.

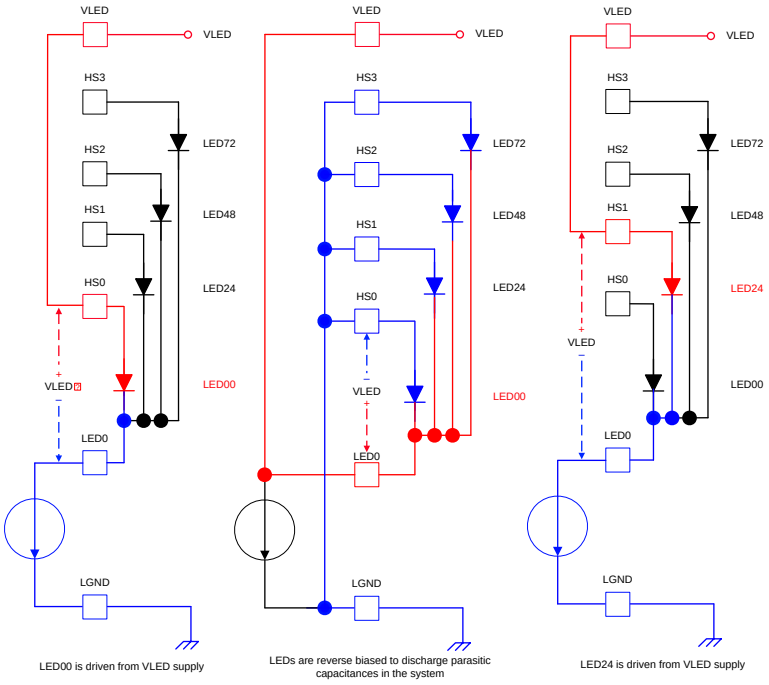

Figure 15. Matrix Ghosting Cancellation

The ghosting cancellation phases and LED driver group turnon delays reduce the maximum PWM on-time for each LED. A 10-kHz LED sequence has a total period of 100 µs. With four LED phases each LED has a maximum on-time of 25 µs. The 150-ns ghosting phase and a 3 clock turnon delay, reduce this on-time to 24.7 µs at 100% LED brightness. This means the 9-bit brightness control results in approximately 48-ns duty cycle steps per brightness LSB.

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7.3.4.3 Sloper

Two optional sloper functions create smooth transitions from one brightness value to another. One sloper operates for master brightness changes, and the second sloper can be assigned to any individual LED or group of LEDs using the LEDxx_slope bits.

Sloper transition time between two brightness values is programmed with register bits master_slope_select[1:0] and matrix_slope_select[1:0]. For 2-ms and 10-ms durations the sloper is linear. For 50-ms and 200-ms durations the sloper uses a curve-bending function to produce a brightness transition that appears visually smoother. Further, a master_slope_en[0] bit is used to disable the function for the master sloper. To disable the matrix sloper, all the LEDxx_slope bits can be set to 0. The sloper_matrix_done and sloper_master_done bits are set once the sloper is complete.

The master sloper may be interrupted with a new brightness change, and it restarts from current brightness and begins sloping to new brightness target. The matrix sloper must finish before being used again for a new brightness level or different group of LEDs. While the matrix sloper is in progress any LEDs that were assigned to the sloper continue to follow the sloper output and are not updated by a new LATCH event. All other registers of LEDs not assigned to an in-progress matrix sloper can be updated and LATCHED normally.

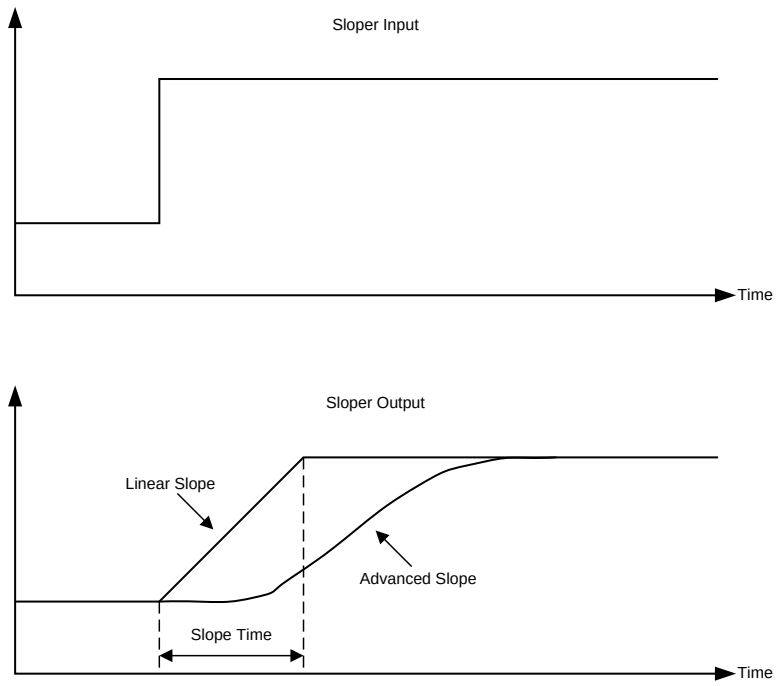

Figure 16. Master Sloper

Table 2, Table 3, and Table 4 show the available sloper settings for the master and matrix sloping functions. Advanced sloping options are intended to create visually smooth brightness transitions while the linear sloping options are intended to soften the load transient for the VLED supply when rapid brightness changes are required.

Table 2. Master Slope Enable

master_slope-en[0]	
0	master sloper disabled
1	master sloper enabled

Table 3. Master Slope Select

master_slope-sel[1:0]	
00	2 ms + adv slope disabled
01	10 ms + adv slope disabled

Table 3. Master Slope Select (continued)

master_slope-sel[1:0]	
10	50 ms + adv slope enabled
11	200 ms + adv slope enabled

Table 4. Matrix Slope Select

matrix_slope-sel[1:0]	
00	2 ms + adv slope disabled
01	10 ms + adv slope disabled
10	50 ms + adv slope enabled
11	200 ms + adv slope enabled

7.3.5 Protection and Fault Detection

The LED171596A includes fault detections for LED-open and LED-short conditions and die overtemperature. Host can monitor the status of the faults via registers and the INT pin. Fault status and interrupt handling is described in Interrupts section.

7.3.5.1 LED Faults

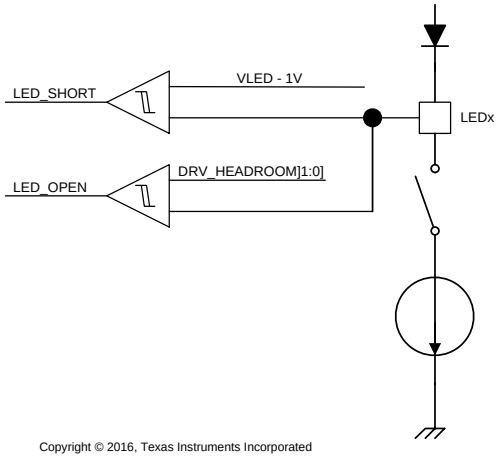

Figure 17. LED-Open, LED-Short Detect Architecture

- Thresholds
  - LED short threshold = (V_{LED} – 1 V) typical
  - LED open threshold = 0.25 V typical (0.25 V, V_{SAT} + 0.25 V, V_{SAT} + 0.5 V_{SAT}, V_{SAT} + 0.75 V programmable with DRV_HEADROOM bits)
- Detection
  - The LED open and short comparators are sampled after a blanking window following the start of the PWM cycle.
  - The output of each comparator is held until latched by fault detection 6 µs after the start of the PWM cycle when pwm_freq_sel = 1.
  - The LED faults are evaluated over a detection window of 16 HS cycles to avoid false fault detection.
    - In order for the LED fault condition to be detected it must be continuously present for one full detection window.
    - Because the fault condition can occur just following the first PWM cycle in a detection window the LED fault detection can vary from 16 to 31 HS cycles (1.55 to 3.1 ms when pwm_freq_sel=1).
  - LED open and short detection only performed when brightness is greater than 10 dec (> 500 ns on-time

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pulse when pwm_freq_sel=1).
  - Ghosting cancellation will be disabled for the phase where shorted LED has been detected and will remain disabled until the LED fault has been cleared.
- Action:
  - LEDs do not disable automatically (user can program brightness to zero)
  - LED_OPEN_INT_EN and LED_SHORT_INT_EN define whether fault/interrupt pin is set (default stored in EPROM bits)
  - Global *LED Short* and *LED Open* bits are set.
  - 96 LED fault signals stored internally and can be read with the LEDXX_XX_OPEN and LEDXX_XX_SHORT registers. Also, a global LED_OPEN and LED_SHORT bit is set when any of the individual bits are set.
  - o LED fault status cleared by writing *CLEAR_LED_OPEN* or *CLEAR_LED_SHORT* bits in the INT_CLEAR register.
    - The correct procedure for clearing faulty LED is to disable the failing LED by setting ledxx_xx_disable bit = 1 in the LEDxx_xx_DISABLE register at least 3.1 ms before clearing the LED fault.

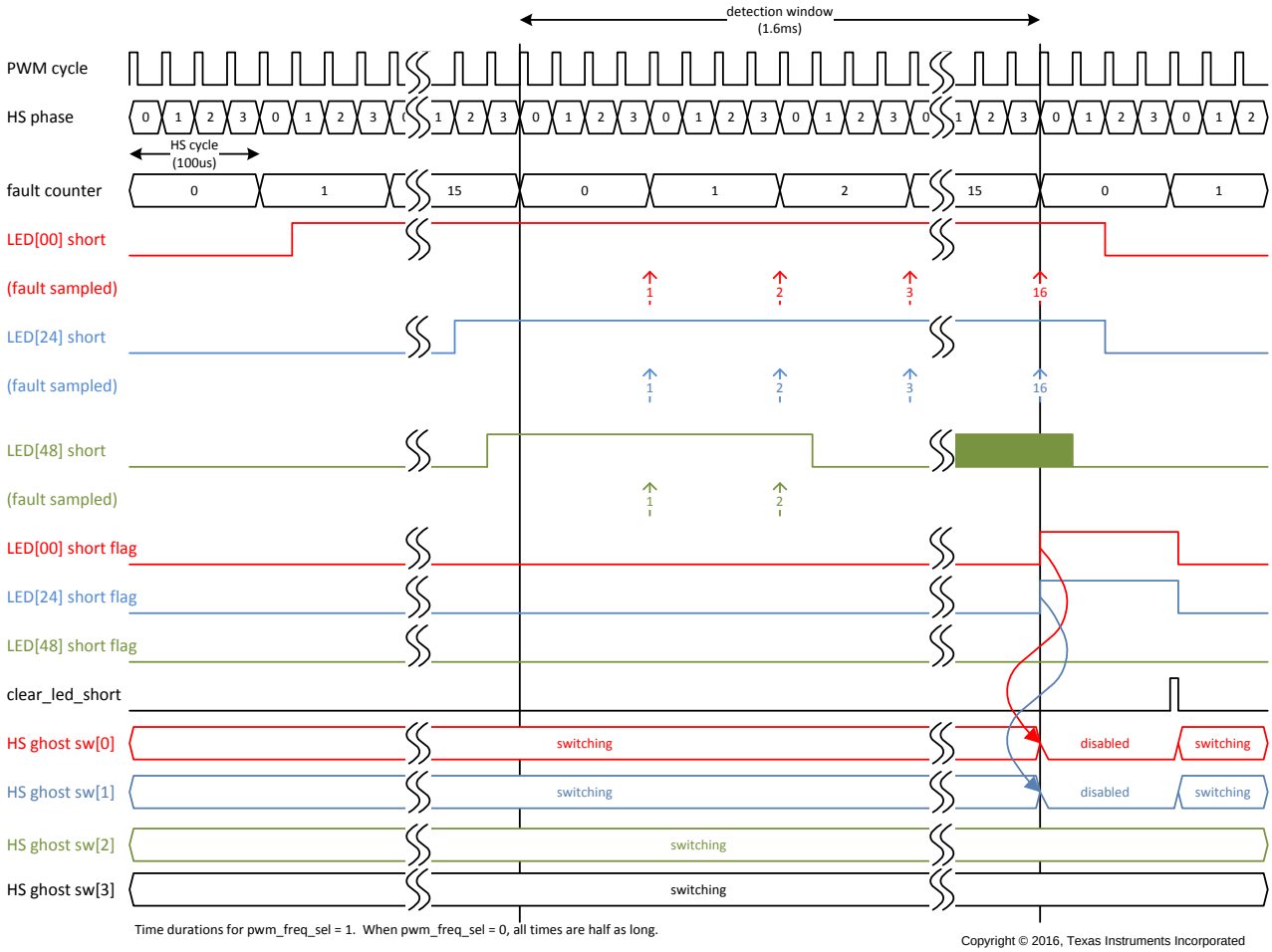

Figure 18. Shorted LED detection timing with automatic ghost cancellation disable

7.3.5.2 Thermal Shutdown

If the die temperature of the LED171596A device reaches the thermal shutdown threshold T_{TSD} (150°C nominal), the LED outputs are forced into shutdown to protect the device from damage. TSD INT_STATUS bit is set. If the MASK_TSD bit is zero then the interrupt pin is also pulled low. The device restarts the LED outputs when temperature drops by T_{TSD_THR} (20°C nominal).

The LED171596A device must not be started up if the ambient temperature is > 130°C. If this condition occurs, the device trips a TSD fault immediately, and the EEPROM is not loaded to prevent data corruption. The INT pin still goes low to indicate a TSD fault but the I^2C and SPI interfaces are not fully operational. Once the temperature drops below the T_{TSD} trip level, the EEPROM is loaded and the device proceeds to STANDBY state and normal operation.

7.4 Device Functional Modes

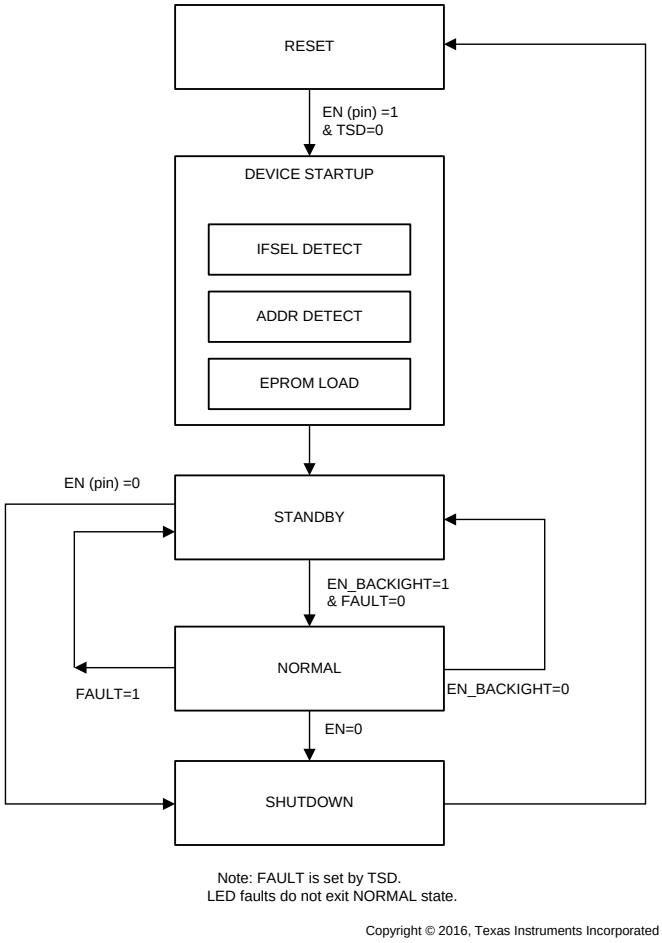

Figure 19. State Machine

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Device Functional Modes (continued)

7.4.1 Reset

The device is in reset when the EN pin is low for $t_{DISABLE}$ time. I^2C/SPI interfaces are not active, and all the LED drivers are disabled.

7.4.2 Device Start-Up

The supplies VDD, VDDIO and VLED should be applied according to where (t1 ≥ t2 ≥ 0 ms) provided that VDD > VDDIO. The timing interval t3 is dependent on the rise time of VLED supply where VLED is up and stable (LED $V_f + V_{SAT}$ volts) prior to EN set high. After EN pin goes high the LED171596A begins device start-up, which takes t_{EN} to complete. This includes checking the state of the address and IFSEL pins and loading the default configuration values from EPROM. If thermal shutdown is asserted the EPROM is not loaded until the TSD condition is cleared. The I^2C and SPI interfaces are not available in this state.

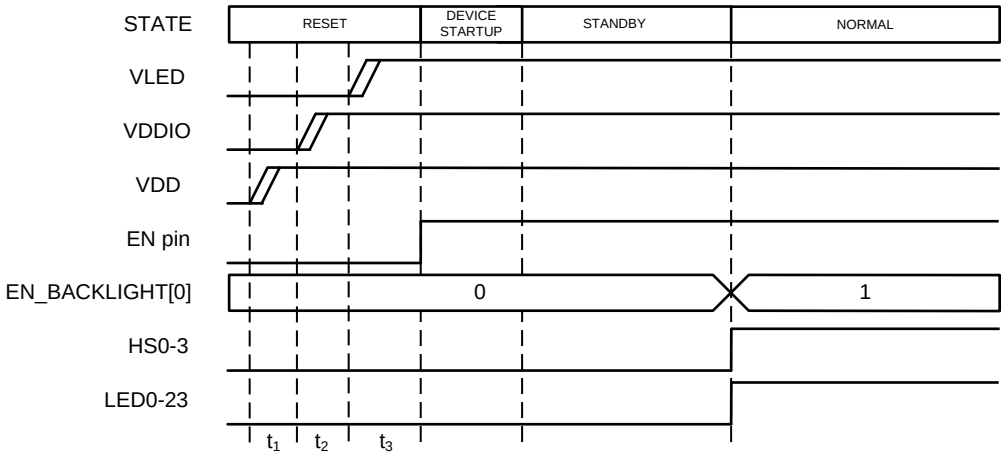

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Figure 20. Start-Up Sequence Diagram

7.4.3 Standby

In standby the LED171596A is ready to be configured by the host with SPI or I^2C interfaces. All user accessible registers can be read or written as applicable. If the EN pin goes low, the device exits to SHUTDOWN state.

7.4.4 Normal

In normal mode the LED matrix sequencer and LED drivers are enabled. LEDs are illuminated in this state, and LED fault detection is active. If the EN_BACKLIGHT bit is written to 0 or if a TSD faults occur, the device exits back to STANDBY state. If the EN pin goes low for $t_{DISABLE}$ time, the device will exit to SHUTDOWN state. All brightness, current and sloper registers may be modified in this state. Avoid changes to matrix sequence configuration registers to avoid any visual artifacts. See *Programming* for more details.

7.4.5 Shutdown

The LED171596A should be shut-down according to where EN_BACKLIGHT (bit) is set low prior to EN pin set low (t1 ≥ t2 ≥ t3 ≥ 0 ms) provided that VDD > VDD_{POR} when EN pin set low. In SHUTDOWN the LED drivers are disabled. The device is shut down and proceeds to RESET state.

Device Functional Modes (continued)

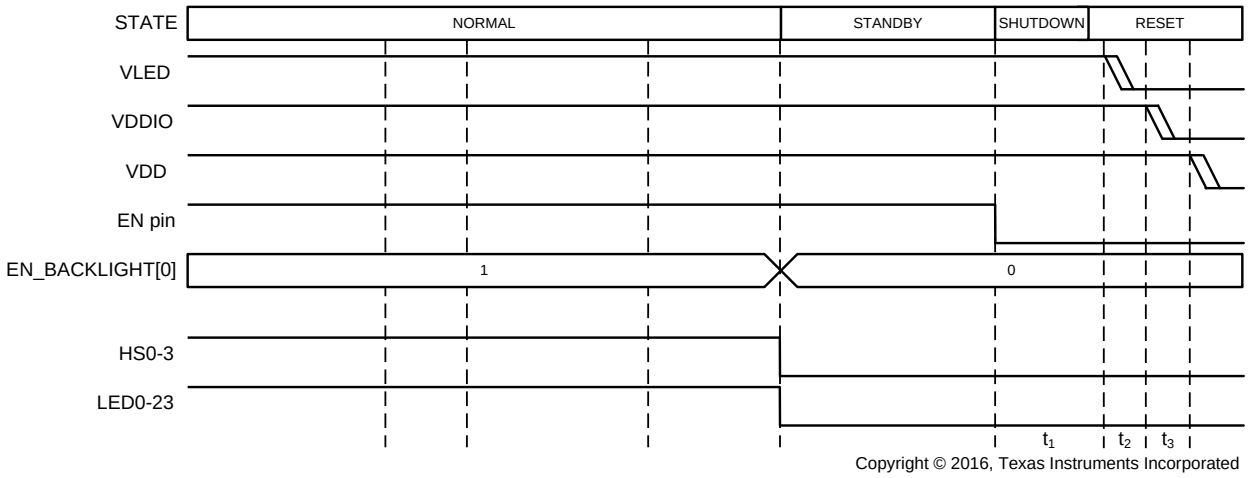

Figure 21. Shut-Down Sequence Diagram

7.5 Programming

7.5.1 Serial Interfaces

The LED171596A supports two serial interfaces: I^2C and 16-bit SPI. Sampling of IFSEL_LATCH pin happens after the rising edge of EN pin. After detection of the selected interface, the IFSEL_LATCH pin can be used to latch written SRAM data to internal processing. The minimum pulse width for LATCH signal is 500 ns. Interface selection for the IFSEL_LATCH pin is:

- 0 – SPI mode
- 1 – I^2C-compatible mode

7.5.1.1 SPI Interface

In SPI mode host can address as many unique LED171596A devices as there are slave select pins on host. The complete register space in LED171596A can be accessed using SPI interface. Rising edge of IFSEL_LATCH pin or LATCH bit are used to latch written SRAM data to internal processing.

The LED171596A is compatible with SPI serial-bus specification and operates as a slave device. The transmission consists of 32-bit write and read cycles. One cycle consists of 15-bit address (9 bits used), 1 read/write (R/W) bit and 16-bit data (9 bits used) to maintain compatibility with16-bit SPI.

The R/W bit high state defines a write cycle and low defines a read cycle. The MISO output is normally in a high-impedance state. When the slave-select pin SS for the device is active (that is, low) the MISO output is pulled low for read only. During write cycle MISO stays in high-impedance state. This allows the host to write data to multiple LED171596A slave devices simultaneously if the SS pin is pulled low on all devices. The address and data bits are transmitted MSB first. The slave-select signal SS must be low during the cycle transmission. SS resets the interface when high, and it has to be taken high between successive cycles, except when using auto-increment mode. Data is clocked in on the rising edge of the SCK clock signal, while data is clocked out on the falling edge of SCK.

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Programming (continued)

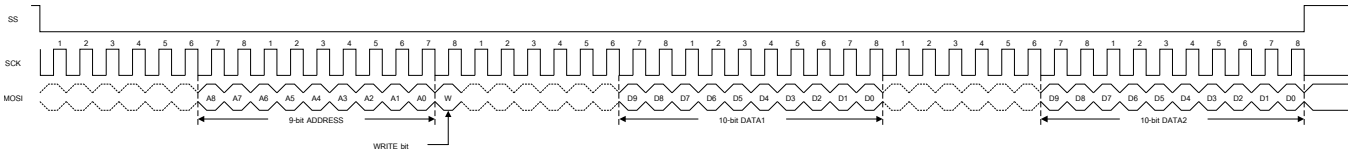

Figure 22. SPI Write

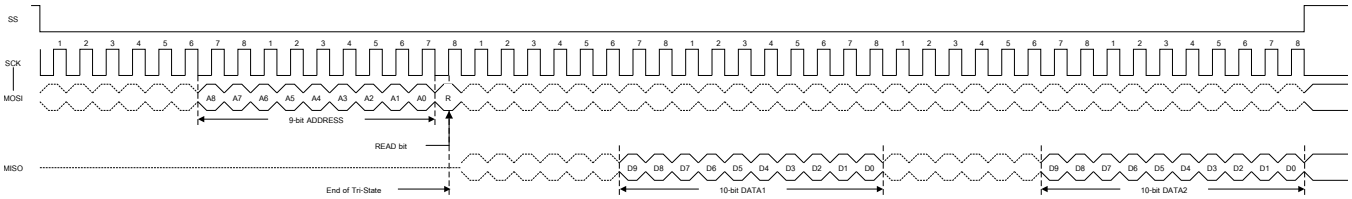

Figure 23. SPI Read

7.5.1.2 I²C-Compatible Interface

Up to three LED171596A slave devices may share the same I²C bus. The first 8 bits of the I²C transaction are divided into bits for the slave ID, one bit for the register address MSB, and the read/write bit. The MISO_ADDR pin is used to select the unique I²C slave address for each device. Every device also uses a single common I²C address so that host can write data to all devices at the same time. This option can be used to write LATCH command to all devices simultaneously.

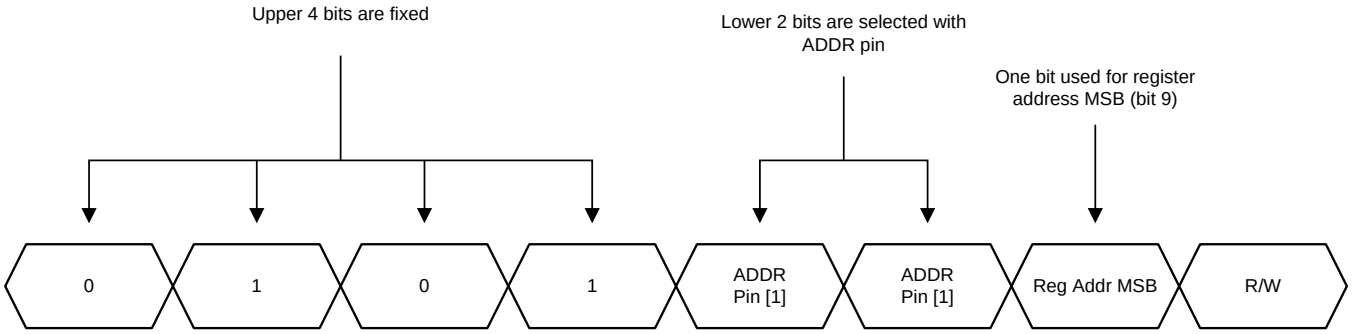

Figure 24. I²C Slave Address Diagram

The LED171596A uses a 6-bit slave ID. The 4 upper bits of the slave ID are fixed to 0101 and the 2 lower bits are defined by the status of the MISO_ADDR pin of each device. The MISO_ADDR pin can be tied to ground, tied to VDDIO, or left unconnected to select between three unique device slave addresses.

Table 5. Slave Addresses

MISO_ADDR STATE	LOWER SLAVE ID BITS	BASE 8-BIT DEVICE ADDRESS
GND	00	50h
VDDIO	01	54h
OPEN	10	58h

This results in three unique slave IDs of 14h (010100), 15h(010101) and 16h (010110). The common slave ID that all devices accept, regardless of MISO_ADDR pin state, is 17h (010111). The common slave ID allows writing the same data to all devices simultaneously, but must not be use for reading. Figure 25 shows how three LED171596A devices can be addressed with the same I²C interface.

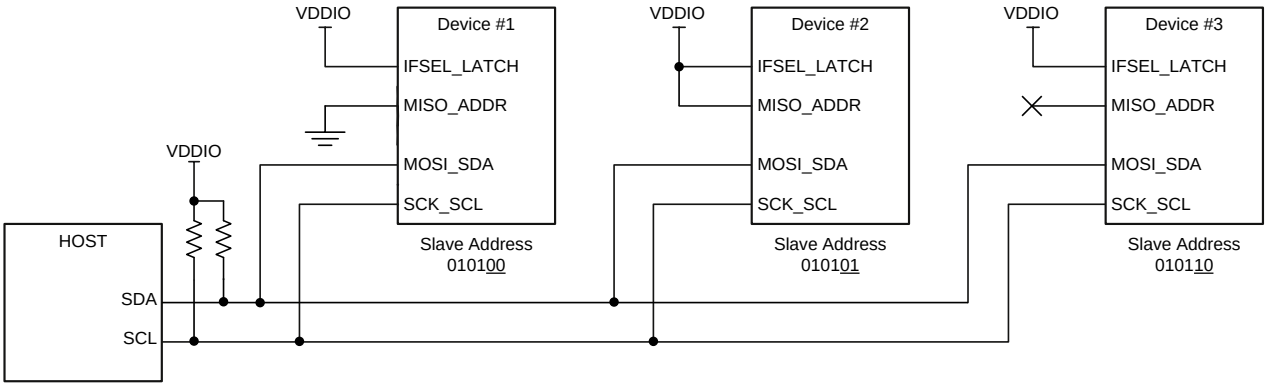

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Figure 25. I²C Addresses Using Three LED171596A Devices

Table 6. I²C ADDRESS Detail Description

UPPER 4 BITS OF SLAVE ID				SLAVE ID BITS FROM ADDR PIN		9-BIT REG ADDR MSB	R/W	8-BIT ADDRESS
0	1	0	1	0	0	0	0	50h
0	1	0	1	0	0	0	1	51h
0	1	0	1	0	0	1	0	52h
0	1	0	1	0	0	1	1	53h
0	1	0	1	0	1	0	0	54h
0	1	0	1	0	1	0	1	55h
0	1	0	1	0	1	1	0	56h
0	1	0	1	0	1	1	1	57h
0	1	0	1	1	0	0	0	58h
0	1	0	1	1	0	0	1	59h
0	1	0	1	1	0	1	0	5Ah
0	1	0	1	1	0	1	1	5Bh
0	1	0	1	1	1	0	0	5Ch
0	1	0	1	1	1	1	0	5Eh
				Common Slave ID Bits				

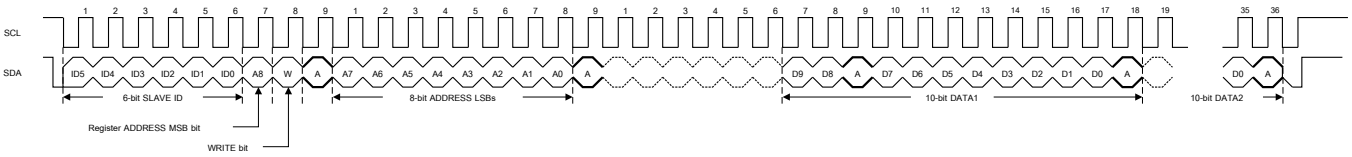

Figure 26. I²C Write

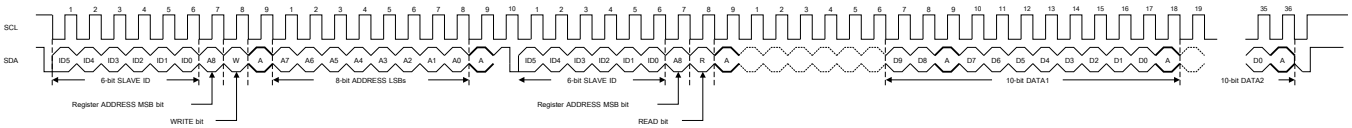

Figure 27. I²C Read

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7.6 Register Maps

7.6.1 LED171596A_MAP Registers

Table 7 lists the memory-mapped registers for the LED171596A_MAP. All register offset addresses not listed in Table 7 should be considered as reserved locations, and the register contents should not be modified.

Table 7. LED171596A_MAP Registers

Offset	Acronym	Register Name	Section
0h	CONFIG_PWM		Go
1h	ENABLES		Go
2h	LATCH		Go
3h	STATUS		Go
4h	INT_STATUS		Go
5h	INT_MASK		Go
6h	INT_CLEAR		Go
8h	LED15_08_OPEN		Go
9h	LED23_16_OPEN		Go
Ah	LED31_24_OPEN		Go
Bh	LED39_32_OPEN		Go
Ch	LED47_40_OPEN		Go
Dh	LED55_48_OPEN		Go
Eh	LED63_56_OPEN		Go
Fh	LED71_64_OPEN		Go
10h	LED79_72_OPEN		Go
11h	LED87_80_OPEN		Go
12h	LED95_88_OPEN		Go
13h	LED07_00_SHORT		Go
14h	LED15_08_SHORT		Go
15h	LED23_16_SHORT		Go
16h	LED31_24_SHORT		Go
17h	LED39_32_SHORT		Go
18h	LED47_40_SHORT		Go
19h	LED55_48_SHORT		Go
1Ah	LED63_56_SHORT		Go
1Bh	LED71_64_SHORT		Go
1Ch	LED79_72_SHORT		Go
1Dh	LED87_80_SHORT		Go
1Eh	LED95_88_SHORT		Go
21h	LED_DRIVER_CONTROL		Go
100h	LED00_CUR		Go
101h	LED01_CUR		Go
102h	LED02_CUR		Go
103h	LED03_CUR		Go
104h	LED04_CUR		Go
105h	LED05_CUR		Go
106h	LED06_CUR		Go
107h	LED07_CUR		Go
108h	LED08_CUR		Go
109h	LED09_CUR		Go
10Ah	LED10_CUR		Go

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Table 7. LED171596A_MAP Registers (continued)

Offset	Acronym	Register Name	Section
10Bh	LED11_CUR		Go
10Ch	LED12_CUR		Go
10Dh	LED13_CUR		Go
10Eh	LED14_CUR		Go
10Fh	LED15_CUR		Go
110h	LED16_CUR		Go
111h	LED17_CUR		Go
112h	LED18_CUR		Go
113h	LED19_CUR		Go
114h	LED20_CUR		Go
115h	LED21_CUR		Go
116h	LED22_CUR		Go
117h	LED23_CUR		Go
118h	LED24_CUR		Go
119h	LED25_CUR		Go
11Ah	LED26_CUR		Go
11Bh	LED27_CUR		Go
11Ch	LED28_CUR		Go
11Dh	LED29_CUR		Go
11Eh	LED30_CUR		Go
11Fh	LED31_CUR		Go
120h	LED32_CUR		Go
121h	LED33_CUR		Go
122h	LED34_CUR		Go
123h	LED35_CUR		Go
124h	LED36_CUR		Go
125h	LED37_CUR		Go
126h	LED38_CUR		Go
127h	LED39_CUR		Go
128h	LED40_CUR		Go
129h	LED41_CUR		Go
12Ah	LED42_CUR		Go
12Bh	LED43_CUR		Go
12Ch	LED44_CUR		Go
12Dh	LED45_CUR		Go
12Eh	LED46_CUR		Go
12Fh	LED47_CUR		Go
130h	LED48_CUR		Go
131h	LED49_CUR		Go
132h	LED50_CUR		Go
133h	LED51_CUR		Go
134h	LED52_CUR		Go
135h	LED53_CUR		Go
136h	LED54_CUR		Go
137h	LED55_CUR		Go
138h	LED56_CUR		Go
139h	LED57_CUR		Go

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Table 7. LED171596A_MAP Registers (continued)

Offset	Acronym	Register Name	Section
13Ah	LED58_CUR		Go
13Bh	LED59_CUR		Go
13Ch	LED60_CUR		Go
13Dh	LED61_CUR		Go
13Eh	LED62_CUR		Go
13Fh	LED63_CUR		Go
140h	LED64_CUR		Go
141h	LED65_CUR		Go
142h	LED66_CUR		Go
143h	LED67_CUR		Go
144h	LED68_CUR		Go
145h	LED69_CUR		Go
146h	LED70_CUR		Go
147h	LED71_CUR		Go
148h	LED72_CUR		Go
149h	LED73_CUR		Go
14Ah	LED74_CUR		Go
14Bh	LED75_CUR		Go
14Ch	LED76_CUR		Go
14Dh	LED77_CUR		Go
14Eh	LED78_CUR		Go
14Fh	LED79_CUR		Go
150h	LED80_CUR		Go
151h	LED81_CUR		Go
152h	LED82_CUR		Go
153h	LED83_CUR		Go
154h	LED84_CUR		Go
155h	LED85_CUR		Go
156h	LED86_CUR		Go
157h	LED87_CUR		Go
158h	LED88_CUR		Go
159h	LED89_CUR		Go
15Ah	LED90_CUR		Go
15Bh	LED91_CUR		Go
15Ch	LED92_CUR		Go
15Dh	LED93_CUR		Go
15Eh	LED94_CUR		Go
15Fh	LED95_CUR		Go
160h	LED00_BRI		Go
161h	LED01_BRI		Go
162h	LED02_BRI		Go
163h	LED03_BRI		Go
164h	LED04_BRI		Go
165h	LED05_BRI		Go
166h	LED06_BRI		Go
167h	LED07_BRI		Go
168h	LED08_BRI		Go

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Table 7. LED171596A_MAP Registers (continued)

Offset	Acronym	Register Name	Section
169h	LED09_BRI		Go
16Ah	LED10_BRI		Go
16Bh	LED11_BRI		Go
16Ch	LED12_BRI		Go
16Dh	LED13_BRI		Go
16Eh	LED14_BRI		Go
16Fh	LED15_BRI		Go
170h	LED16_BRI		Go
171h	LED17_BRI		Go
172h	LED18_BRI		Go
173h	LED19_BRI		Go
174h	LED20_BRI		Go
175h	LED21_BRI		Go
176h	LED22_BRI		Go
177h	LED23_BRI		Go
178h	LED24_BRI		Go
179h	LED25_BRI		Go
17Ah	LED26_BRI		Go
17Bh	LED27_BRI		Go
17Ch	LED28_BRI		Go
17Dh	LED29_BRI		Go
17Eh	LED30_BRI		Go
17Fh	LED31_BRI		Go
180h	LED32_BRI		Go
181h	LED33_BRI		Go
182h	LED34_BRI		Go
183h	LED35_BRI		Go
184h	LED36_BRI		Go
185h	LED37_BRI		Go
186h	LED38_BRI		Go
187h	LED39_BRI		Go
188h	LED40_BRI		Go
189h	LED41_BRI		Go
18Ah	LED42_BRI		Go
18Bh	LED43_BRI		Go
18Ch	LED44_BRI		Go
18Dh	LED45_BRI		Go
18Eh	LED46_BRI		Go
18Fh	LED47_BRI		Go
190h	LED48_BRI		Go
191h	LED49_BRI		Go
192h	LED50_BRI		Go
193h	LED51_BRI		Go
194h	LED52_BRI		Go
195h	LED53_BRI		Go
196h	LED54_BRI		Go
197h	LED55_BRI		Go

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Table 7. LED171596A_MAP Registers (continued)

Offset	Acronym	Register Name	Section
198h	LED56_BRI		Go
199h	LED57_BRI		Go
19Ah	LED58_BRI		Go
19Bh	LED59_BRI		Go
19Ch	LED60_BRI		Go
19Dh	LED61_BRI		Go
19Eh	LED62_BRI		Go
19Fh	LED63_BRI		Go
1A0h	LED64_BRI		Go
1A1h	LED65_BRI		Go
1A2h	LED66_BRI		Go
1A3h	LED67_BRI		Go
1A4h	LED68_BRI		Go
1A5h	LED69_BRI		Go
1A6h	LED70_BRI		Go
1A7h	LED71_BRI		Go
1A8h	LED72_BRI		Go
1A9h	LED73_BRI		Go
1AAh	LED74_BRI		Go
1ABh	LED75_BRI		Go
1ACh	LED76_BRI		Go
1ADh	LED77_BRI		Go
1AEh	LED78_BRI		Go
1AFh	LED79_BRI		Go
1B0h	LED80_BRI		Go
1B1h	LED81_BRI		Go
1B2h	LED82_BRI		Go
1B3h	LED83_BRI		Go
1B4h	LED84_BRI		Go
1B5h	LED85_BRI		Go
1B6h	LED86_BRI		Go
1B7h	LED87_BRI		Go
1B8h	LED88_BRI		Go
1B9h	LED89_BRI		Go
1BAh	LED90_BRI		Go
1BBh	LED91_BRI		Go
1BCh	LED92_BRI		Go
1BDh	LED93_BRI		Go
1BEh	LED94_BRI		Go
1BFh	LED95_BRI		Go
1C0h	MASTER_BRI		Go
1C1h	LED07_00_DISABLE		Go
1C2h	LED15_08_DISABLE		Go
1C3h	LED23_16_DISABLE		Go
1C4h	LED31_24_DISABLE		Go
1C5h	LED39_32_DISABLE		Go
1C6h	LED47_40_DISABLE		Go

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Table 7. LED171596A_MAP Registers (continued)

Offset	Acronym	Register Name	Section
1C7h	LED55_48_DISABLE		Go
1C8h	LED63_56_DISABLE		Go
1C9h	LED71_64_DISABLE		Go
1CAh	LED79_72_DISABLE		Go
1CBh	LED87_80_DISABLE		Go
1CCh	LED95_88_DISABLE		Go
1CDh	SLOPERS_CONFIG		Go
1CEh	SLOPER_TARGET		Go
1CFh	LED07_00_SLOPE		Go
1D0h	LED15_08_SLOPE		Go
1D1h	LED23_16_SLOPE		Go
1D2h	LED31_24_SLOPE		Go
1D3h	LED39_32_SLOPE		Go
1D4h	LED47_40_SLOPE		Go
1D5h	LED55_48_SLOPE		Go
1D6h	LED63_56_SLOPE		Go
1D7h	LED71_64_SLOPE		Go
1D8h	LED79_72_SLOPE		Go
1D9h	LED87_80_SLOPE		Go
1DAh	LED95_88_SLOPE		Go
1DBh	LEDGRP1_BRI		Go
1DCh	LEDGRP2_BRI		Go
1DDh	LEDGRP3_BRI		Go
1DEh	LED04_00_GRPSEL		Go
1DFh	LED09_05_GRPSEL		Go
1E0h	LED14_10_GRPSEL		Go
1E1h	LED19_15_GRPSEL		Go
1E2h	LED24_20_GRPSEL		Go
1E3h	LED29_25_GRPSEL		Go
1E4h	LED34_30_GRPSEL		Go
1E5h	LED39_35_GRPSEL		Go
1E6h	LED44_40_GRPSEL		Go
1E7h	LED49_45_GRPSEL		Go
1E8h	LED54_50_GRPSEL		Go
1E9h	LED59_55_GRPSEL		Go
1EAh	LED64_60_GRPSEL		Go
1EBh	LED69_65_GRPSEL		Go
1ECh	LED74_70_GRPSEL		Go
1EDh	LED79_75_GRPSEL		Go
1EEh	LED84_80_GRPSEL		Go
1EFh	LED89_85_GRPSEL		Go
1F0h	LED94_90_GRPSEL		Go
1F1h	LED95_GRPSEL		Go

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7.6.1.1 CONFIG_PWM Register (Address = 0h) [reset = 1Fh]

CONFIG_PWM is shown in Figure 28 and described in Table 8.

Return to Summary Table.

Figure 28. CONFIG_PWM Register

15	14	13	12	11	10	9	8
RESERVED						pwm_input_edge_sel	pwm_input_hysteresis
R/W-0h						R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
pwm_input_hysteresis		enable_pwm_detector	pwm_freq_sel	pwm_phase_shift_config		RESERVED	
R/W-0h		R/W-0h	R/W-1h	R/W-3h		R/W-3h	

Table 8. CONFIG_PWM Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	
9	pwm_input_edge_sel	R/W	0h	PWM period is measured: 0 - from rising edge to rising edge 1 - from falling edge to falling edge
8-6	pwm_input_hysteresis	R/W	0h	PWM hysteresis selection sets the minimum allowable change to the input. Hysteresis is monitoring direction of change and if direction is changing then hysteresis will apply. If a smaller change is detected to opposite direction, it is ignored. With hysteresis the constant changing between two brightness values is avoided if there is small jitter in the input signal. Hysteresis is selected with pwm_input_hysteresis bits in register CONFIG_PWM. Hysteresis is calculated from pwm detector 16-bit output value. Using a higher hysteresis setting is recommended with high PWM input frequencies.; Hysteresis (decimal), calculated from 16 bit value 000 - off 001 - 15 010 - 31 011 - 63 100 - 127 101 - 255 110 - 511 111 - 1023
5	enable_pwm_detector	R/W	0h	PWM input detector enable
4	pwm_freq_sel	R/W	1h	PWM Frequency selector: 0 - 20 kHz 1 - 10 kHz
3-2	pwm_phase_shift_config	R/W	3h	PWM phaseshifting 00 - off 01 - 1 clock cycles 10 - 2 clock cycles 11 - 3 clock cycles
1-0	RESERVED	R/W	3h	NOTE: When updating other fields in this register the 2 lsb reset value must be preserved!

7.6.1.2 ENABLES Register (Address = 1h) [reset = 0h]

ENABLES is shown in Figure 29 and described in Table 9.

Return to Summary Table.

Figure 29. ENABLES Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							en_backlight
R/W-0h							R/W-0h

Table 9. ENABLES Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R/W	0h	
0	en_backlight	R/W	0h	Enable LEDs 0 - LED driving disabled. Device stays in STANDBY state. 1 - LED driving enabled.

7.6.1.3 LATCH Register (Address = 2h) [reset = 0h]

LATCH is shown in Figure 30 and described in Table 10.

Return to Summary Table.

Figure 30. LATCH Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							latch
R/W-0h							R-0/WSelfClr-0h

Table 10. LATCH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R/W	0h	
0	latch	R-0/WSelfClr	0h	Latch SRAM data. Writing 1 generates a latch pulse. Read returns always 0.

7.6.1.4 STATUS Register (Address = 3h) [reset = 0h]

STATUS is shown in Figure 31 and described in Table 11.

Return to Summary Table.

Figure 31. STATUS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					slope_matrix_busy	slope_master_busy	latch_busy
R-0h					R-0h	R-0h	R-0h

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Table 11. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0h	
2	slope_matrix_busy	R	0h	Matrix sloper status 0 - Matrix sloper ready 1 - Matrix sloper busy
1	slope_master_busy	R	0h	Master sloper status 0 - Master sloper ready 1 - Master sloper busy
0	latch_busy	R	0h	SRAM data latching status 0 - SRAM data latching ready 1 - SRAM data latching busy

7.6.1.5 INT_STATUS Register (Address = 4h) [reset = 0h]

INT_STATUS is shown in Figure 32 and described in Table 12.

Return to Summary Table.

Interrupt status bits are set by events and cleared by bits in INT_CLEAR register. Status bits show if an event has occurred since the last clearing. Start of an unmasked event sets the INT pin. If INT pin is cleared while an event is active, it stays cleared until some other event starts.

Figure 32. INT_STATUS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	led_open	led_short	RESERVED	tsd	slope_matrix_done	slope_master_done	latch_done
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 12. INT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0h	
6	led_open	R	0h	LED open fault interrupt status
5	led_short	R	0h	LED short fault interrupt status
4	RESERVED	R	0h	
3	tsd	R	0h	Thermal shutdown interrupt status
2	slope_matrix_done	R	0h	Matrix sloper interrupt status
1	slope_master_done	R	0h	Master sloper interrupt status
0	latch_done	R	0h	SRAM latching interrupt status

7.6.1.6 INT_MASK Register (Address = 5h) [reset = 17h]

INT_MASK is shown in Figure 33 and described in Table 13.

Return to Summary Table.

Interrupt mask bits mask the event for INT pin. Interrupt status bits are not affected by mask bits.

Figure 33. INT_MASK Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	mask_led_open	mask_led_short	RESERVED	mask_tsd	mask_slope_matrix_done	mask_slope_master_done	mask_latch_done
R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-1h	R/W-1h

Table 13. INT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R/W	0h	
6	mask_led_open	R/W	0h	LED open fault interrupt mask
5	mask_led_short	R/W	0h	LED short fault interrupt mask
4	RESERVED	R/W	1h	
3	mask_tsd	R/W	0h	Thermal shutdown interrupt mask
2	mask_slope_matrix_done	R/W	1h	Matrix sloper interrupt mask
1	mask_slope_master_done	R/W	1h	Master sloper interrupt mask
0	mask_latch_done	R/W	1h	SRAM latching interrupt mask

7.6.1.7 INT_CLEAR Register (Address = 6h) [reset = 0h]

INT_CLEAR is shown in Figure 34 and described in Table 14.

Return to Summary Table.

Interrupt clear bits. Writing 1 generates a clear pulse. Read returns always 0.

Figure 34. INT_CLEAR Register

15	14	13	12	11	10	9	8
RESERVED							clear_int_pin
R/W-0h							R-0/WSelfClr-0h
7	6	5	4	3	2	1	0
RESERVED	clear_led_open	clear_led_short	RESERVED	clear_tsd	clear_slope_matrix_done	clear_slope_master_done	clear_latch_done
R/W-0h	R-0/WSelfClr-0h	R-0/WSelfClr-0h	R/W-0h	R-0/WSelfClr-0h	R-0/WSelfClr-0h	R-0/WSelfClr-0h	R-0/WSelfClr-0h

Table 14. INT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8	clear_int_pin	R-0/WSelfClr	0h	INT pin clear
7	RESERVED	R/W	0h	
6	clear_led_open	R-0/WSelfClr	0h	LED open fault interrupt status clear
5	clear_led_short	R-0/WSelfClr	0h	LED short fault interrupt status clear
4	RESERVED	R/W-0h	0h	
3	clear_tsd	R-0/WSelfClr	0h	Thermal shutdown interrupt status clear

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Table 14. INT_CLEAR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	clear_slope_matrix_done	R-0/WSelfClr	0h	Matrix sloper interrupt status clear
1	clear_slope_master_done	R-0/WSelfClr	0h	Master sloper interrupt status clear
0	clear_latch_done	R-0/WSelfClr	0h	SRAM latching interrupt status clear

7.6.1.8 LED07_00_OPEN Register (Address = 7h) [reset = 0h]

LED07_00_OPEN is shown in Figure 35 and described in Table 15.

Return to Summary Table.

LED open fault status bits are set by starting LED open fault and cleared by clear_led_open bit in INT_CLEAR register. Status bits show if LED open fault has occurred since the last clearing.

Figure 35. LED07_00_OPEN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
led07_00_open							
R-0h							

Table 15. LED07_00_OPEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led07_00_open	R	0h	Open fault status for LEDs 0-7 (First matrix phase)

7.6.1.9 LED15_08_OPEN Register (Address = 8h) [reset = 0h]

LED15_08_OPEN is shown in Figure 36 and described in Table 16.

Return to Summary Table.

LED open fault status bits are set by starting LED open fault and cleared by clear_led_open bit in INT_CLEAR register. Status bits show if LED open fault has occurred since the last clearing.

Figure 36. LED15_08_OPEN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
led15_08_open							
R-0h							

Table 16. LED15_08_OPEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led15_08_open	R	0h	Open fault status for LEDs 8-15 (First matrix phase)

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7.6.1.10 LED23_16_OPEN Register (Address = 9h) [reset = 0h]

LED23_16_OPEN is shown in Figure 37 and described in Table 17.

Return to Summary Table.

LED open fault status bits are set by starting LED open fault and cleared by clear_led_open bit in INT_CLEAR register. Status bits show if LED open fault has occurred since the last clearing.

Figure 37. LED23_16_OPEN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
led23_16_open							
R-0h							

Table 17. LED23_16_OPEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led23_16_open	R	0h	Open fault status for LEDs 16-23 (First matrix phase)

7.6.1.11 LED31_24_OPEN Register (Address = Ah) [reset = 0h]

LED31_24_OPEN is shown in Figure 38 and described in Table 18.

Return to Summary Table.

LED open fault status bits are set by starting LED open fault and cleared by clear_led_open bit in INT_CLEAR register. Status bits show if LED open fault has occurred since the last clearing.

Figure 38. LED31_24_OPEN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
led31_24_open							
R-0h							

Table 18. LED31_24_OPEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led31_24_open	R	0h	Open fault status for LEDs 24-31 (Second matrix phase)

7.6.1.12 LED39_32_OPEN Register (Address = Bh) [reset = 0h]

LED39_32_OPEN is shown in Figure 39 and described in Table 19.

Return to Summary Table.

LED open fault status bits are set by starting LED open fault and cleared by clear_led_open bit in INT_CLEAR register. Status bits show if LED open fault has occurred since the last clearing.

Figure 39. LED39_32_OPEN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

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7	6	5	4	3	2	1	0
led39_32_open							
R-0h							

Table 19. LED39_32_OPEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led39_32_open	R	0h	Open fault status for LEDs 32-39 (Second matrix phase)

7.6.1.13 LED47_40_OPEN Register (Address = Ch) [reset = 0h]

LED47_40_OPEN is shown in Figure 40 and described in Table 20.

Return to Summary Table.

LED open fault status bits are set by starting LED open fault and cleared by clear_led_open bit in INT_CLEAR register. Status bits show if LED open fault has occurred since the last clearing.

Figure 40. LED47_40_OPEN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
led47_40_open							
R-0h							

Table 20. LED47_40_OPEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led47_40_open	R	0h	Open fault status for LEDs 40-47 (Second matrix phase)

7.6.1.14 LED55_48_OPEN Register (Address = Dh) [reset = 0h]

LED55_48_OPEN is shown in Figure 41 and described in Table 21.

Return to Summary Table.

LED open fault status bits are set by starting LED open fault and cleared by clear_led_open bit in INT_CLEAR register. Status bits show if LED open fault has occurred since the last clearing.

Figure 41. LED55_48_OPEN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
led55_48_open							
R-0h							

Table 21. LED55_48_OPEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led55_48_open	R	0h	Open fault status for LEDs 48-55 (Third matrix phase)

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7.6.1.15 LED63_56_OPEN Register (Address = Eh) [reset = 0h]

LED63_56_OPEN is shown in Figure 42 and described in Table 22.

Return to Summary Table.

LED open fault status bits are set by starting LED open fault and cleared by clear_led_open bit in INT_CLEAR register. Status bits show if LED open fault has occurred since the last clearing.

Figure 42. LED63_56_OPEN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
led63_56_open							
R-0h							

Table 22. LED63_56_OPEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led63_56_open	R	0h	Open fault status for LEDs 56-63 (Third matrix phase)

7.6.1.16 LED71_64_OPEN Register (Address = Fh) [reset = 0h]

LED71_64_OPEN is shown in Figure 43 and described in Table 23.

Return to Summary Table.

LED open fault status bits are set by starting LED open fault and cleared by clear_led_open bit in INT_CLEAR register. Status bits show if LED open fault has occurred since the last clearing.

Figure 43. LED71_64_OPEN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
led71_64_open							
R-0h							

Table 23. LED71_64_OPEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led71_64_open	R	0h	Open fault status for LEDs 64-71 (Third matrix phase)

7.6.1.17 LED79_72_OPEN Register (Address = 10h) [reset = 0h]

LED79_72_OPEN is shown in Figure 44 and described in Table 24.

Return to Summary Table.

LED open fault status bits are set by starting LED open fault and cleared by clear_led_open bit in INT_CLEAR register. Status bits show if LED open fault has occurred since the last clearing.

Figure 44. LED79_72_OPEN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

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7	6	5	4	3	2	1	0
led79_72_open							
R-0h							

Table 24. LED79_72_OPEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led79_72_open	R	0h	Open fault status for LEDs 72-79 (Fourth matrix phase)

7.6.1.18 LED87_80_OPEN Register (Address = 11h) [reset = 0h]

LED87_80_OPEN is shown in Figure 45 and described in Table 25.

Return to Summary Table.

LED open fault status bits are set by starting LED open fault and cleared by clear_led_open bit in INT_CLEAR register. Status bits show if LED open fault has occurred since the last clearing.

Figure 45. LED87_80_OPEN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
led87_80_open							
R-0h							

Table 25. LED87_80_OPEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led87_80_open	R	0h	Open fault status for LEDs 80-87 (Fourth matrix phase)

7.6.1.19 LED95_88_OPEN Register (Address = 12h) [reset = 0h]

LED95_88_OPEN is shown in Figure 46 and described in Table 26.

Return to Summary Table.

LED open fault status bits are set by starting LED open fault and cleared by clear_led_open bit in INT_CLEAR register. Status bits show if LED open fault has occurred since the last clearing.

Figure 46. LED95_88_OPEN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
led95_88_open							
R-0h							

Table 26. LED95_88_OPEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led95_88_open	R	0h	Open fault status for LEDs 88-95 (Fourth matrix phase)

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7.6.1.20 LED07_00_SHORT Register (Address = 13h) [reset = 0h]

LED07_00_SHORT is shown in Figure 47 and described in Table 27.

Return to Summary Table.

LED short fault status bits are set by starting LED short fault and cleared by clear_led_short bit in INT_CLEAR register. Status bits show if LED short fault has occurred since the last clearing.

Figure 47. LED07_00_SHORT Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
led07_00_short							
R-0h							

Table 27. LED07_00_SHORT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led07_00_short	R	0h	Short fault status for LEDs 0-7 (First matrix phase)

7.6.1.21 LED15_08_SHORT Register (Address = 14h) [reset = 0h]

LED15_08_SHORT is shown in Figure 48 and described in Table 28.

Return to Summary Table.

LED short fault status bits are set by starting LED short fault and cleared by clear_led_short bit in INT_CLEAR register. Status bits show if LED short fault has occurred since the last clearing.

Figure 48. LED15_08_SHORT Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
led15_08_short							
R-0h							

Table 28. LED15_08_SHORT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led15_08_short	R	0h	Short fault status for LEDs 8-15 (First matrix phase)

7.6.1.22 LED23_16_SHORT Register (Address = 15h) [reset = 0h]

LED23_16_SHORT is shown in Figure 49 and described in Table 29.

Return to Summary Table.

LED short fault status bits are set by starting LED short fault and cleared by clear_led_short bit in INT_CLEAR register. Status bits show if LED short fault has occurred since the last clearing.

Figure 49. LED23_16_SHORT Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

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7	6	5	4	3	2	1	0
led23_16_short							
R-0h							

Table 29. LED23_16_SHORT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led23_16_short	R	0h	Short fault status for LEDs 16-23 (First matrix phase)

7.6.1.23 LED31_24_SHORT Register (Address = 16h) [reset = 0h]

LED31_24_SHORT is shown in Figure 50 and described in Table 30.

Return to Summary Table.

LED short fault status bits are set by starting LED short fault and cleared by clear_led_short bit in INT_CLEAR register. Status bits show if LED short fault has occurred since the last clearing.

Figure 50. LED31_24_SHORT Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
led31_24_short							
R-0h							

Table 30. LED31_24_SHORT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led31_24_short	R	0h	Short fault status for LEDs 24-31 (Second matrix phase)

7.6.1.24 LED39_32_SHORT Register (Address = 17h) [reset = 0h]

LED39_32_SHORT is shown in Figure 51 and described in Table 31.

Return to Summary Table.

LED short fault status bits are set by starting LED short fault and cleared by clear_led_short bit in INT_CLEAR register. Status bits show if LED short fault has occurred since the last clearing.

Figure 51. LED39_32_SHORT Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
led39_32_short							
R-0h							

Table 31. LED39_32_SHORT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led39_32_short	R	0h	Short fault status for LEDs 32-39 (Second matrix phase)

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7.6.1.25 LED47_40_SHORT Register (Address = 18h) [reset = 0h]

LED47_40_SHORT is shown in Figure 52 and described in Table 32.

Return to Summary Table.

LED short fault status bits are set by starting LED short fault and cleared by clear_led_short bit in INT_CLEAR register. Status bits show if LED short fault has occurred since the last clearing.

Figure 52. LED47_40_SHORT Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
led47_40_short							
R-0h							

Table 32. LED47_40_SHORT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led47_40_short	R	0h	Short fault status for LEDs 40-47 (Second matrix phase)

7.6.1.26 LED55_48_SHORT Register (Address = 19h) [reset = 0h]

LED55_48_SHORT is shown in Figure 53 and described in Table 33.

Return to Summary Table.

LED short fault status bits are set by starting LED short fault and cleared by clear_led_short bit in INT_CLEAR register. Status bits show if LED short fault has occurred since the last clearing.

Figure 53. LED55_48_SHORT Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
led55_48_short							
R-0h							

Table 33. LED55_48_SHORT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led55_48_short	R	0h	Short fault status for LEDs 48-55 (Third matrix phase)

7.6.1.27 LED63_56_SHORT Register (Address = 1Ah) [reset = 0h]

LED63_56_SHORT is shown in Figure 54 and described in Table 34.

Return to Summary Table.

LED short fault status bits are set by starting LED short fault and cleared by clear_led_short bit in INT_CLEAR register. Status bits show if LED short fault has occurred since the last clearing.

Figure 54. LED63_56_SHORT Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

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7	6	5	4	3	2	1	0
led63_56_short							
R-0h							

Table 34. LED63_56_SHORT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led63_56_short	R	0h	Short fault status for LEDs 56-63 (Third matrix phase)

7.6.1.28 LED71_64_SHORT Register (Address = 1Bh) [reset = 0h]

LED71_64_SHORT is shown in Figure 55 and described in Table 35.

Return to Summary Table.

LED short fault status bits are set by starting LED short fault and cleared by clear_led_short bit in INT_CLEAR register. Status bits show if LED short fault has occurred since the last clearing.

Figure 55. LED71_64_SHORT Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
led71_64_short							
R-0h							

Table 35. LED71_64_SHORT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led71_64_short	R	0h	Short fault status for LEDs 64-71 (Third matrix phase)

7.6.1.29 LED79_72_SHORT Register (Address = 1Ch) [reset = 0h]

LED79_72_SHORT is shown in Figure 56 and described in Table 36.

Return to Summary Table.

LED short fault status bits are set by starting LED short fault and cleared by clear_led_short bit in INT_CLEAR register. Status bits show if LED short fault has occurred since the last clearing.

Figure 56. LED79_72_SHORT Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
led79_72_short							
R-0h							

Table 36. LED79_72_SHORT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led79_72_short	R	0h	Short fault status for LEDs 72-79 (Fourth matrix phase)

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7.6.1.30 LED87_80_SHORT Register (Address = 1Dh) [reset = 0h]

LED87_80_SHORT is shown in Figure 57 and described in Table 37.

Return to Summary Table.

LED short fault status bits are set by starting LED short fault and cleared by clear_led_short bit in INT_CLEAR register. Status bits show if LED short fault has occurred since the last clearing.

Figure 57. LED87_80_SHORT Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
led87_80_short							
R-0h							

Table 37. LED87_80_SHORT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led87_80_short	R	0h	Short fault status for LEDs 80-87 (Fourth matrix phase)

7.6.1.31 LED95_88_SHORT Register (Address = 1Eh) [reset = 0h]

LED95_88_SHORT is shown in Figure 58 and described in Table 38.

Return to Summary Table.

LED short fault status bits are set by starting LED short fault and cleared by clear_led_short bit in INT_CLEAR register. Status bits show if LED short fault has occurred since the last clearing.

Figure 58. LED95_88_SHORT Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
led95_88_short							
R-0h							

Table 38. LED95_88_SHORT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	
7-0	led95_88_short	R	0h	Short fault status for LEDs 88-95 (Fourth matrix phase)

7.6.1.32 LED_DRIVER_CONTROL Register (Address = 21h) [reset = 34h]

LED_DRIVER_CONTROL is shown in Figure 59 and described in Table 39.

Return to Summary Table.

Figure 59. LED_DRIVER_CONTROL Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		hs_en_ghost_cancel	drv_en_ghost_level		drv_en_ghost_cancel	drv_headroom	

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R/W-0h	R/W-1h	R/W-2h	R/W-1h	R/W-0h

Table 39. LED_DRIVER_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R/W	0h	
5	hs_en_ghost_cancel	R/W	1h	Enable for high side switch ghost cancellation 0 - disabled 1 - enabled
4-3	drv_en_ghost_level	R/W	2h	Ghost cancellation strength select 00 - disabled 01 - weakest 10 - medium 11 - strongest
2	drv_en_ghost_cancel	R/W	1h	Enable for LED driver ghost cancellation 0 - disabled 1 - enabled
1-0	drv_headroom	R/W	0h	LED driver headroom select 00 - 250mV 01 - 0.9 * Vsat + 250mV 10 - 0.9 * Vsat + 500mV 11 - 0.9 * Vsat + 750mV

7.6.1.33 LED00_CUR Register (Address = 100h) [reset = CCh]

LED00_CUR is shown in Figure 60 and described in Table 40.

Return to Summary Table.

Figure 60. LED00_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led00_cur							
R/W-CCh							

Table 40. LED00_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led00_cur	R/W	CCh	LED00 driver linear current value

7.6.1.34 LED01_CUR Register (Address = 101h) [reset = CCh]

LED01_CUR is shown in Figure 61 and described in Table 41.

Return to Summary Table.

Figure 61. LED01_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led01_cur							
R/W-CCh							

Table 41. LED01_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led01_cur	R/W	CCh	LED01 driver linear current value

7.6.1.35 LED02_CUR Register (Address = 102h) [reset = CCh]

LED02_CUR is shown in Figure 62 and described in Table 42.

Return to Summary Table.

Figure 62. LED02_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led02_cur							
R/W-CCh							

Table 42. LED02_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led02_cur	R/W	CCh	LED02 driver linear current value

7.6.1.36 LED03_CUR Register (Address = 103h) [reset = CCh]

LED03_CUR is shown in Figure 63 and described in Table 43.

Return to Summary Table.

Figure 63. LED03_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led03_cur							
R/W-CCh							

Table 43. LED03_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led03_cur	R/W	CCh	LED03 driver linear current value

7.6.1.37 LED04_CUR Register (Address = 104h) [reset = CCh]

LED04_CUR is shown in Figure 64 and described in Table 44.

Return to Summary Table.

Figure 64. LED04_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							

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7	6	5	4	3	2	1	0
led04_cur							
R/W-CCh							

Table 44. LED04_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led04_cur	R/W	CCh	LED04 driver linear current value

7.6.1.38 LED05_CUR Register (Address = 105h) [reset = CCh]

LED05_CUR is shown in Figure 65 and described in Table 45.

Return to Summary Table.

Figure 65. LED05_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led05_cur							
R/W-CCh							

Table 45. LED05_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led05_cur	R/W	CCh	LED05 driver linear current value

7.6.1.39 LED06_CUR Register (Address = 106h) [reset = CCh]

LED06_CUR is shown in Figure 66 and described in Table 46.

Return to Summary Table.

Figure 66. LED06_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led06_cur							
R/W-CCh							

Table 46. LED06_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led06_cur	R/W	CCh	LED06 driver linear current value

7.6.1.40 LED07_CUR Register (Address = 107h) [reset = CCh]

LED07_CUR is shown in Figure 67 and described in Table 47.

Return to Summary Table.

Figure 67. LED07_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led07_cur							
R/W-CCh							

Table 47. LED07_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led07_cur	R/W	CCh	LED07 driver linear current value

7.6.1.41 LED08_CUR Register (Address = 108h) [reset = CCh]

LED08_CUR is shown in Figure 68 and described in Table 48.

Return to Summary Table.

Figure 68. LED08_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led08_cur							
R/W-CCh							

Table 48. LED08_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led08_cur	R/W	CCh	LED08 driver linear current value

7.6.1.42 LED09_CUR Register (Address = 109h) [reset = CCh]

LED09_CUR is shown in Figure 69 and described in Table 49.

Return to Summary Table.

Figure 69. LED09_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led09_cur							
R/W-CCh							

Table 49. LED09_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led09_cur	R/W	CCh	LED09 driver linear current value

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7.6.1.43 LED10_CUR Register (Address = 10Ah) [reset = CCh]

LED10_CUR is shown in Figure 70 and described in Table 50.

Return to Summary Table.

Figure 70. LED10_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led10_cur							
R/W-CCh							

Table 50. LED10_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led10_cur	R/W	CCh	LED10 driver linear current value

7.6.1.44 LED11_CUR Register (Address = 10Bh) [reset = CCh]

LED11_CUR is shown in Figure 71 and described in Table 51.

Return to Summary Table.

Figure 71. LED11_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led11_cur							
R/W-CCh							

Table 51. LED11_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led11_cur	R/W	CCh	LED11 driver linear current value

7.6.1.45 LED12_CUR Register (Address = 10Ch) [reset = CCh]

LED12_CUR is shown in Figure 72 and described in Table 52.

Return to Summary Table.

Figure 72. LED12_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led12_cur							
R/W-CCh							

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Table 52. LED12_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led12_cur	R/W	CCh	LED12 driver linear current value

7.6.1.46 LED13_CUR Register (Address = 10Dh) [reset = CCh]

LED13_CUR is shown in Figure 73 and described in Table 53.

Return to Summary Table.

Figure 73. LED13_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led13_cur							
R/W-CCh							

Table 53. LED13_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led13_cur	R/W	CCh	LED13 driver linear current value

7.6.1.47 LED14_CUR Register (Address = 10Eh) [reset = CCh]

LED14_CUR is shown in Figure 74 and described in Table 54.

Return to Summary Table.

Figure 74. LED14_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led14_cur							
R/W-CCh							

Table 54. LED14_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led14_cur	R/W	CCh	LED14 driver linear current value

7.6.1.48 LED15_CUR Register (Address = 10Fh) [reset = CCh]

LED15_CUR is shown in Figure 75 and described in Table 55.

Return to Summary Table.

Figure 75. LED15_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							

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7	6	5	4	3	2	1	0
led15_cur							
R/W-CCh							

Table 55. LED15_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led15_cur	R/W	CCh	LED15 driver linear current value

7.6.1.49 LED16_CUR Register (Address = 110h) [reset = CCh]

LED16_CUR is shown in Figure 76 and described in Table 56.

Return to Summary Table.

Figure 76. LED16_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led16_cur							
R/W-CCh							

Table 56. LED16_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led16_cur	R/W	CCh	LED16 driver linear current value

7.6.1.50 LED17_CUR Register (Address = 111h) [reset = CCh]

LED17_CUR is shown in Figure 77 and described in Table 57.

Return to Summary Table.

Figure 77. LED17_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led17_cur							
R/W-CCh							

Table 57. LED17_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led17_cur	R/W	CCh	LED17 driver linear current value

7.6.1.51 LED18_CUR Register (Address = 112h) [reset = CCh]

LED18_CUR is shown in Figure 78 and described in Table 58.

Return to Summary Table.

Figure 78. LED18_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led18_cur							
R/W-CCh							

Table 58. LED18_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led18_cur	R/W	CCh	LED18 driver linear current value

7.6.1.52 LED19_CUR Register (Address = 113h) [reset = CCh]

LED19_CUR is shown in Figure 79 and described in Table 59.

Return to Summary Table.

Figure 79. LED19_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led19_cur							
R/W-CCh							

Table 59. LED19_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led19_cur	R/W	CCh	LED19 driver linear current value

7.6.1.53 LED20_CUR Register (Address = 114h) [reset = CCh]

LED20_CUR is shown in Figure 80 and described in Table 60.

Return to Summary Table.

Figure 80. LED20_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led20_cur							
R/W-CCh							

Table 60. LED20_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led20_cur	R/W	CCh	LED20 driver linear current value

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7.6.1.54 LED21_CUR Register (Address = 115h) [reset = CCh]

LED21_CUR is shown in Figure 81 and described in Table 61.

Return to Summary Table.

Figure 81. LED21_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led21_cur							
R/W-CCh							

Table 61. LED21_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led21_cur	R/W	CCh	LED21 driver linear current value

7.6.1.55 LED22_CUR Register (Address = 116h) [reset = CCh]

LED22_CUR is shown in Figure 82 and described in Table 62.

Return to Summary Table.

Figure 82. LED22_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led22_cur							
R/W-CCh							

Table 62. LED22_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led22_cur	R/W	CCh	LED22 driver linear current value

7.6.1.56 LED23_CUR Register (Address = 117h) [reset = CCh]

LED23_CUR is shown in Figure 83 and described in Table 63.

Return to Summary Table.

Figure 83. LED23_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led23_cur							
R/W-CCh							

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Table 63. LED23_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led23_cur	R/W	CCh	LED23 driver linear current value

7.6.1.57 LED24_CUR Register (Address = 118h) [reset = CCh]

LED24_CUR is shown in Figure 84 and described in Table 64.

Return to Summary Table.

Figure 84. LED24_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led24_cur							
R/W-CCh							

Table 64. LED24_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led24_cur	R/W	CCh	LED24 driver linear current value

7.6.1.58 LED25_CUR Register (Address = 119h) [reset = CCh]

LED25_CUR is shown in Figure 85 and described in Table 65.

Return to Summary Table.

Figure 85. LED25_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led25_cur							
R/W-CCh							

Table 65. LED25_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led25_cur	R/W	CCh	LED25 driver linear current value

7.6.1.59 LED26_CUR Register (Address = 11Ah) [reset = CCh]

LED26_CUR is shown in Figure 86 and described in Table 66.

Return to Summary Table.

Figure 86. LED26_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							

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7	6	5	4	3	2	1	0
led26_cur							
R/W-CCh							

Table 66. LED26_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led26_cur	R/W	CCh	LED26 driver linear current value

7.6.1.60 LED27_CUR Register (Address = 11Bh) [reset = CCh]

LED27_CUR is shown in Figure 87 and described in Table 67.

Return to Summary Table.

Figure 87. LED27_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led27_cur							
R/W-CCh							

Table 67. LED27_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led27_cur	R/W	CCh	LED27 driver linear current value

7.6.1.61 LED28_CUR Register (Address = 11Ch) [reset = CCh]

LED28_CUR is shown in Figure 88 and described in Table 68.

Return to Summary Table.

Figure 88. LED28_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led28_cur							
R/W-CCh							

Table 68. LED28_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led28_cur	R/W	CCh	LED28 driver linear current value

7.6.1.62 LED29_CUR Register (Address = 11Dh) [reset = CCh]

LED29_CUR is shown in Figure 89 and described in Table 69.

Return to Summary Table.

Figure 89. LED29_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led29_cur							
R/W-CCh							

Table 69. LED29_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led29_cur	R/W	CCh	LED29 driver linear current value

7.6.1.63 LED30_CUR Register (Address = 11Eh) [reset = CCh]

LED30_CUR is shown in Figure 90 and described in Table 70.

Return to Summary Table.

Figure 90. LED30_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led30_cur							
R/W-CCh							

Table 70. LED30_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led30_cur	R/W	CCh	LED30 driver linear current value

7.6.1.64 LED31_CUR Register (Address = 11Fh) [reset = CCh]

LED31_CUR is shown in Figure 91 and described in Table 71.

Return to Summary Table.

Figure 91. LED31_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led31_cur							
R/W-CCh							

Table 71. LED31_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led31_cur	R/W	CCh	LED31 driver linear current value

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7.6.1.65 LED32_CUR Register (Address = 120h) [reset = CCh]

LED32_CUR is shown in Figure 92 and described in Table 72.

Return to Summary Table.

Figure 92. LED32_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led32_cur							
R/W-CCh							

Table 72. LED32_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led32_cur	R/W	CCh	LED32 driver linear current value

7.6.1.66 LED33_CUR Register (Address = 121h) [reset = CCh]

LED33_CUR is shown in Figure 93 and described in Table 73.

Return to Summary Table.

Figure 93. LED33_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led33_cur							
R/W-CCh							

Table 73. LED33_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led33_cur	R/W	CCh	LED33 driver linear current value

7.6.1.67 LED34_CUR Register (Address = 122h) [reset = CCh]

LED34_CUR is shown in Figure 94 and described in Table 74.

Return to Summary Table.

Figure 94. LED34_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led34_cur							
R/W-CCh							

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Table 74. LED34_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led34_cur	R/W	CCh	LED34 driver linear current value

7.6.1.68 LED35_CUR Register (Address = 123h) [reset = CCh]

LED35_CUR is shown in Figure 95 and described in Table 75.

Return to Summary Table.

Figure 95. LED35_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led35_cur							
R/W-CCh							

Table 75. LED35_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led35_cur	R/W	CCh	LED35 driver linear current value

7.6.1.69 LED36_CUR Register (Address = 124h) [reset = CCh]

LED36_CUR is shown in Figure 96 and described in Table 76.

Return to Summary Table.

Figure 96. LED36_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led36_cur							
R/W-CCh							

Table 76. LED36_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led36_cur	R/W	CCh	LED36 driver linear current value

7.6.1.70 LED37_CUR Register (Address = 125h) [reset = CCh]

LED37_CUR is shown in Figure 97 and described in Table 77.

Return to Summary Table.

Figure 97. LED37_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							

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7	6	5	4	3	2	1	0
led37_cur							
R/W-CCh							

Table 77. LED37_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led37_cur	R/W	CCh	LED37 driver linear current value

7.6.1.71 LED38_CUR Register (Address = 126h) [reset = CCh]

LED38_CUR is shown in Figure 98 and described in Table 78.

Return to Summary Table.

Figure 98. LED38_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led38_cur							
R/W-CCh							

Table 78. LED38_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led38_cur	R/W	CCh	LED38 driver linear current value

7.6.1.72 LED39_CUR Register (Address = 127h) [reset = CCh]

LED39_CUR is shown in Figure 99 and described in Table 79.

Return to Summary Table.

Figure 99. LED39_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led39_cur							
R/W-CCh							

Table 79. LED39_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led39_cur	R/W	CCh	LED39 driver linear current value

7.6.1.73 LED40_CUR Register (Address = 128h) [reset = CCh]

LED40_CUR is shown in Figure 100 and described in Table 80.

Return to Summary Table.

Figure 100. LED40_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led40_cur							
R/W-CCh							

Table 80. LED40_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led40_cur	R/W	CCh	LED40 driver linear current value

7.6.1.74 LED41_CUR Register (Address = 129h) [reset = CCh]

LED41_CUR is shown in Figure 101 and described in Table 81.

Return to Summary Table.

Figure 101. LED41_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led41_cur							
R/W-CCh							

Table 81. LED41_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led41_cur	R/W	CCh	LED41 driver linear current value

7.6.1.75 LED42_CUR Register (Address = 12Ah) [reset = CCh]

LED42_CUR is shown in Figure 102 and described in Table 82.

Return to Summary Table.

Figure 102. LED42_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led42_cur							
R/W-CCh							

Table 82. LED42_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led42_cur	R/W	CCh	LED42 driver linear current value

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7.6.1.76 LED43_CUR Register (Address = 12Bh) [reset = CCh]

LED43_CUR is shown in Figure 103 and described in Table 83.

Return to Summary Table.

Figure 103. LED43_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led43_cur							
R/W-CCh							

Table 83. LED43_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led43_cur	R/W	CCh	LED43 driver linear current value

7.6.1.77 LED44_CUR Register (Address = 12Ch) [reset = CCh]

LED44_CUR is shown in Figure 104 and described in Table 84.

Return to Summary Table.

Figure 104. LED44_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led44_cur							
R/W-CCh							

Table 84. LED44_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led44_cur	R/W	CCh	LED44 driver linear current value

7.6.1.78 LED45_CUR Register (Address = 12Dh) [reset = CCh]

LED45_CUR is shown in Figure 105 and described in Table 85.

Return to Summary Table.

Figure 105. LED45_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led45_cur							
R/W-CCh							

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Table 85. LED45_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led45_cur	R/W	CCh	LED45 driver linear current value

7.6.1.79 LED46_CUR Register (Address = 12Eh) [reset = CCh]

LED46_CUR is shown in Figure 106 and described in Table 86.

Return to Summary Table.

Figure 106. LED46_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led46_cur							
R/W-CCh							

Table 86. LED46_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led46_cur	R/W	CCh	LED46 driver linear current value

7.6.1.80 LED47_CUR Register (Address = 12Fh) [reset = CCh]

LED47_CUR is shown in Figure 107 and described in Table 87.

Return to Summary Table.

Figure 107. LED47_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led47_cur							
R/W-CCh							

Table 87. LED47_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led47_cur	R/W	CCh	LED47 driver linear current value

7.6.1.81 LED48_CUR Register (Address = 130h) [reset = CCh]

LED48_CUR is shown in Figure 108 and described in Table 88.

Return to Summary Table.

Figure 108. LED48_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							

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7	6	5	4	3	2	1	0
led48_cur							
R/W-CCh							

Table 88. LED48_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led48_cur	R/W	CCh	LED48 driver linear current value

7.6.1.82 LED49_CUR Register (Address = 131h) [reset = CCh]

LED49_CUR is shown in Figure 109 and described in Table 89.

Return to Summary Table.

Figure 109. LED49_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led49_cur							
R/W-CCh							

Table 89. LED49_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led49_cur	R/W	CCh	LED49 driver linear current value

7.6.1.83 LED50_CUR Register (Address = 132h) [reset = CCh]

LED50_CUR is shown in Figure 110 and described in Table 90.

Return to Summary Table.

Figure 110. LED50_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led50_cur							
R/W-CCh							

Table 90. LED50_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led50_cur	R/W	CCh	LED50 driver linear current value

7.6.1.84 LED51_CUR Register (Address = 133h) [reset = CCh]

LED51_CUR is shown in Figure 111 and described in Table 91.

Return to Summary Table.

Figure 111. LED51_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led51_cur							
R/W-CCh							

Table 91. LED51_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led51_cur	R/W	CCh	LED51 driver linear current value

7.6.1.85 LED52_CUR Register (Address = 134h) [reset = CCh]

LED52_CUR is shown in Figure 112 and described in Table 92.

Return to Summary Table.

Figure 112. LED52_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led52_cur							
R/W-CCh							

Table 92. LED52_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led52_cur	R/W	CCh	LED52 driver linear current value

7.6.1.86 LED53_CUR Register (Address = 135h) [reset = CCh]

LED53_CUR is shown in Figure 113 and described in Table 93.

Return to Summary Table.

Figure 113. LED53_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led53_cur							
R/W-CCh							

Table 93. LED53_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led53_cur	R/W	CCh	LED53 driver linear current value

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7.6.1.87 LED54_CUR Register (Address = 136h) [reset = CCh]

LED54_CUR is shown in Figure 114 and described in Table 94.

Return to Summary Table.

Figure 114. LED54_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led54_cur							
R/W-CCh							

Table 94. LED54_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led54_cur	R/W	CCh	LED54 driver linear current value

7.6.1.88 LED55_CUR Register (Address = 137h) [reset = CCh]

LED55_CUR is shown in Figure 115 and described in Table 95.

Return to Summary Table.

Figure 115. LED55_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led55_cur							
R/W-CCh							

Table 95. LED55_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led55_cur	R/W	CCh	LED55 driver linear current value

7.6.1.89 LED56_CUR Register (Address = 138h) [reset = CCh]

LED56_CUR is shown in Figure 116 and described in Table 96.

Return to Summary Table.

Figure 116. LED56_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led56_cur							
R/W-CCh							

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Table 96. LED56_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led56_cur	R/W	CCh	LED56 driver linear current value

7.6.1.90 LED57_CUR Register (Address = 139h) [reset = CCh]

LED57_CUR is shown in Figure 117 and described in Table 97.

Return to Summary Table.

Figure 117. LED57_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led57_cur							
R/W-CCh							

Table 97. LED57_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led57_cur	R/W	CCh	LED57 driver linear current value

7.6.1.91 LED58_CUR Register (Address = 13Ah) [reset = CCh]

LED58_CUR is shown in Figure 118 and described in Table 98.

Return to Summary Table.

Figure 118. LED58_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led58_cur							
R/W-CCh							

Table 98. LED58_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led58_cur	R/W	CCh	LED58 driver linear current value

7.6.1.92 LED59_CUR Register (Address = 13Bh) [reset = CCh]

LED59_CUR is shown in Figure 119 and described in Table 99.

Return to Summary Table.

Figure 119. LED59_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							

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7	6	5	4	3	2	1	0
led59_cur							
R/W-CCh							

Table 99. LED59_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led59_cur	R/W	CCh	LED59 driver linear current value

7.6.1.93 LED60_CUR Register (Address = 13Ch) [reset = CCh]

LED60_CUR is shown in Figure 120 and described in Table 100.

Return to Summary Table.

Figure 120. LED60_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led60_cur							
R/W-CCh							

Table 100. LED60_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led60_cur	R/W	CCh	LED60 driver linear current value

7.6.1.94 LED61_CUR Register (Address = 13Dh) [reset = CCh]

LED61_CUR is shown in Figure 121 and described in Table 101.

Return to Summary Table.

Figure 121. LED61_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led61_cur							
R/W-CCh							

Table 101. LED61_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led61_cur	R/W	CCh	LED61 driver linear current value

7.6.1.95 LED62_CUR Register (Address = 13Eh) [reset = CCh]

LED62_CUR is shown in Figure 122 and described in Table 102.

Return to Summary Table.

Figure 122. LED62_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led62_cur							
R/W-CCh							

Table 102. LED62_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led62_cur	R/W	CCh	LED62 driver linear current value

7.6.1.96 LED63_CUR Register (Address = 13Fh) [reset = CCh]

LED63_CUR is shown in Figure 123 and described in Table 103.

Return to Summary Table.

Figure 123. LED63_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led63_cur							
R/W-CCh							

Table 103. LED63_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led63_cur	R/W	CCh	LED63 driver linear current value

7.6.1.97 LED64_CUR Register (Address = 140h) [reset = CCh]

LED64_CUR is shown in Figure 124 and described in Table 104.

Return to Summary Table.

Figure 124. LED64_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led64_cur							
R/W-CCh							

Table 104. LED64_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led64_cur	R/W	CCh	LED64 driver linear current value

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7.6.1.98 LED65_CUR Register (Address = 141h) [reset = CCh]

LED65_CUR is shown in Figure 125 and described in Table 105.

Return to Summary Table.

Figure 125. LED65_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led65_cur							
R/W-CCh							

Table 105. LED65_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led65_cur	R/W	CCh	LED65 driver linear current value

7.6.1.99 LED66_CUR Register (Address = 142h) [reset = CCh]

LED66_CUR is shown in Figure 126 and described in Table 106.

Return to Summary Table.

Figure 126. LED66_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led66_cur							
R/W-CCh							

Table 106. LED66_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led66_cur	R/W	CCh	LED66 driver linear current value

7.6.1.100 LED67_CUR Register (Address = 143h) [reset = CCh]

LED67_CUR is shown in Figure 127 and described in Table 107.

Return to Summary Table.

Figure 127. LED67_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led67_cur							
R/W-CCh							

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Table 107. LED67_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led67_cur	R/W	CCh	LED67 driver linear current value

7.6.1.101 LED68_CUR Register (Address = 144h) [reset = CCh]

LED68_CUR is shown in Figure 128 and described in Table 108.

Return to Summary Table.

Figure 128. LED68_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led68_cur							
R/W-CCh							

Table 108. LED68_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led68_cur	R/W	CCh	LED68 driver linear current value

7.6.1.102 LED69_CUR Register (Address = 145h) [reset = CCh]

LED69_CUR is shown in Figure 129 and described in Table 109.

Return to Summary Table.

Figure 129. LED69_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led69_cur							
R/W-CCh							

Table 109. LED69_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led69_cur	R/W	CCh	LED69 driver linear current value

7.6.1.103 LED70_CUR Register (Address = 146h) [reset = CCh]

LED70_CUR is shown in Figure 130 and described in Table 110.

Return to Summary Table.

Figure 130. LED70_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							

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7	6	5	4	3	2	1	0
led70_cur							
R/W-CCh							

Table 110. LED70_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led70_cur	R/W	CCh	LED70 driver linear current value

7.6.1.104 LED71_CUR Register (Address = 147h) [reset = CCh]

LED71_CUR is shown in Figure 131 and described in Table 111.

Return to Summary Table.

Figure 131. LED71_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led71_cur							
R/W-CCh							

Table 111. LED71_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led71_cur	R/W	CCh	LED71 driver linear current value

7.6.1.105 LED72_CUR Register (Address = 148h) [reset = CCh]

LED72_CUR is shown in Figure 132 and described in Table 112.

Return to Summary Table.

Figure 132. LED72_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led72_cur							
R/W-CCh							

Table 112. LED72_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led72_cur	R/W	CCh	LED72 driver linear current value

7.6.1.106 LED73_CUR Register (Address = 149h) [reset = CCh]

LED73_CUR is shown in Figure 133 and described in Table 113.

Return to Summary Table.

Figure 133. LED73_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led73_cur							
R/W-CCh							

Table 113. LED73_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led73_cur	R/W	CCh	LED73 driver linear current value

7.6.1.107 LED74_CUR Register (Address = 14Ah) [reset = CCh]

LED74_CUR is shown in Figure 134 and described in Table 114.

Return to Summary Table.

Figure 134. LED74_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led74_cur							
R/W-CCh							

Table 114. LED74_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led74_cur	R/W	CCh	LED74 driver linear current value

7.6.1.108 LED75_CUR Register (Address = 14Bh) [reset = CCh]

LED75_CUR is shown in Figure 135 and described in Table 115.

Return to Summary Table.

Figure 135. LED75_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led75_cur							
R/W-CCh							

Table 115. LED75_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led75_cur	R/W	CCh	LED75 driver linear current value

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7.6.1.109 LED76_CUR Register (Address = 14Ch) [reset = CCh]

LED76_CUR is shown in Figure 136 and described in Table 116.

Return to Summary Table.

Figure 136. LED76_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led76_cur							
R/W-CCh							

Table 116. LED76_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led76_cur	R/W	CCh	LED76 driver linear current value

7.6.1.110 LED77_CUR Register (Address = 14Dh) [reset = CCh]

LED77_CUR is shown in Figure 137 and described in Table 117.

Return to Summary Table.

Figure 137. LED77_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led77_cur							
R/W-CCh							

Table 117. LED77_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led77_cur	R/W	CCh	LED77 driver linear current value

7.6.1.111 LED78_CUR Register (Address = 14Eh) [reset = CCh]

LED78_CUR is shown in Figure 138 and described in Table 118.

Return to Summary Table.

Figure 138. LED78_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led78_cur							
R/W-CCh							

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Table 118. LED78_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led78_cur	R/W	CCh	LED78 driver linear current value

7.6.1.112 LED79_CUR Register (Address = 14Fh) [reset = CCh]

LED79_CUR is shown in Figure 139 and described in Table 119.

Return to Summary Table.

Figure 139. LED79_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led79_cur							
R/W-CCh							

Table 119. LED79_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led79_cur	R/W	CCh	LED79 driver linear current value

7.6.1.113 LED80_CUR Register (Address = 150h) [reset = CCh]

LED80_CUR is shown in Figure 140 and described in Table 120.

Return to Summary Table.

Figure 140. LED80_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led80_cur							
R/W-CCh							

Table 120. LED80_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led80_cur	R/W	CCh	LED80 driver linear current value

7.6.1.114 LED81_CUR Register (Address = 151h) [reset = CCh]

LED81_CUR is shown in Figure 141 and described in Table 121.

Return to Summary Table.

Figure 141. LED81_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							

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7	6	5	4	3	2	1	0
led81_cur							
R/W-CCh							

Table 121. LED81_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led81_cur	R/W	CCh	LED81 driver linear current value

7.6.1.115 LED82_CUR Register (Address = 152h) [reset = CCh]

LED82_CUR is shown in Figure 142 and described in Table 122.

Return to Summary Table.

Figure 142. LED82_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led82_cur							
R/W-CCh							

Table 122. LED82_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led82_cur	R/W	CCh	LED82 driver linear current value

7.6.1.116 LED83_CUR Register (Address = 153h) [reset = CCh]

LED83_CUR is shown in Figure 143 and described in Table 123.

Return to Summary Table.

Figure 143. LED83_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led83_cur							
R/W-CCh							

Table 123. LED83_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led83_cur	R/W	CCh	LED83 driver linear current value

7.6.1.117 LED84_CUR Register (Address = 154h) [reset = CCh]

LED84_CUR is shown in Figure 144 and described in Table 124.

Return to Summary Table.

Figure 144. LED84_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led84_cur							
R/W-CCh							

Table 124. LED84_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led84_cur	R/W	CCh	LED84 driver linear current value

7.6.1.118 LED85_CUR Register (Address = 155h) [reset = CCh]

LED85_CUR is shown in Figure 145 and described in Table 125.

Return to Summary Table.

Figure 145. LED85_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led85_cur							
R/W-CCh							

Table 125. LED85_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led85_cur	R/W	CCh	LED85 driver linear current value

7.6.1.119 LED86_CUR Register (Address = 156h) [reset = CCh]

LED86_CUR is shown in Figure 146 and described in Table 126.

Return to Summary Table.

Figure 146. LED86_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led86_cur							
R/W-CCh							

Table 126. LED86_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led86_cur	R/W	CCh	LED86 driver linear current value

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7.6.1.120 LED87_CUR Register (Address = 157h) [reset = CCh]

LED87_CUR is shown in Figure 147 and described in Table 127.

Return to Summary Table.

Figure 147. LED87_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led87_cur							
R/W-CCh							

Table 127. LED87_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led87_cur	R/W	CCh	LED87 driver linear current value

7.6.1.121 LED88_CUR Register (Address = 158h) [reset = CCh]

LED88_CUR is shown in Figure 148 and described in Table 128.

Return to Summary Table.

Figure 148. LED88_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led88_cur							
R/W-CCh							

Table 128. LED88_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led88_cur	R/W	CCh	LED88 driver linear current value

7.6.1.122 LED89_CUR Register (Address = 159h) [reset = CCh]

LED89_CUR is shown in Figure 149 and described in Table 129.

Return to Summary Table.

Figure 149. LED89_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led89_cur							
R/W-CCh							

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Table 129. LED89_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led89_cur	R/W	CCh	LED89 driver linear current value

7.6.1.123 LED90_CUR Register (Address = 15Ah) [reset = CCh]

LED90_CUR is shown in Figure 150 and described in Table 130.

Return to Summary Table.

Figure 150. LED90_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led90_cur							
R/W-CCh							

Table 130. LED90_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led90_cur	R/W	CCh	LED90 driver linear current value

7.6.1.124 LED91_CUR Register (Address = 15Bh) [reset = CCh]

LED91_CUR is shown in Figure 151 and described in Table 131.

Return to Summary Table.

Figure 151. LED91_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led91_cur							
R/W-CCh							

Table 131. LED91_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led91_cur	R/W	CCh	LED91 driver linear current value

7.6.1.125 LED92_CUR Register (Address = 15Ch) [reset = CCh]

LED92_CUR is shown in Figure 152 and described in Table 132.

Return to Summary Table.

Figure 152. LED92_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							

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7	6	5	4	3	2	1	0
led92_cur							
R/W-CCh							

Table 132. LED92_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led92_cur	R/W	CCh	LED92 driver linear current value

7.6.1.126 LED93_CUR Register (Address = 15Dh) [reset = CCh]

LED93_CUR is shown in Figure 153 and described in Table 133.

Return to Summary Table.

Figure 153. LED93_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led93_cur							
R/W-CCh							

Table 133. LED93_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led93_cur	R/W	CCh	LED93 driver linear current value

7.6.1.127 LED94_CUR Register (Address = 15Eh) [reset = CCh]

LED94_CUR is shown in Figure 154 and described in Table 134.

Return to Summary Table.

Figure 154. LED94_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led94_cur							
R/W-CCh							

Table 134. LED94_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led94_cur	R/W	CCh	LED94 driver linear current value

7.6.1.128 LED95_CUR Register (Address = 15Fh) [reset = CCh]

LED95_CUR is shown in Figure 155 and described in Table 135.

Return to Summary Table.

Figure 155. LED95_CUR Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led95_cur							
R/W-CCh							

Table 135. LED95_CUR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led95_cur	R/W	CCh	LED95 driver linear current value

7.6.1.129 LED00_BRI Register (Address = 160h) [reset = 1FFh]

LED00_BRI is shown in Figure 156 and described in Table 136.

Return to Summary Table.

Figure 156. LED00_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led00_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led00_bri							
R/W-1FFh							

Table 136. LED00_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led00_bri	R/W	1FFh	PWM Brightness of LED00

7.6.1.130 LED01_BRI Register (Address = 161h) [reset = 1FFh]

LED01_BRI is shown in Figure 157 and described in Table 137.

Return to Summary Table.

Figure 157. LED01_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led01_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led01_bri							
R/W-1FFh							

Table 137. LED01_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led01_bri	R/W	1FFh	PWM Brightness of LED01

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7.6.1.131 LED02_BRI Register (Address = 162h) [reset = 1FFh]

LED02_BRI is shown in Figure 158 and described in Table 138.

Return to Summary Table.

Figure 158. LED02_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led02_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led02_bri							
R/W-1FFh							

Table 138. LED02_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led02_bri	R/W	1FFh	PWM Brightness of LED02

7.6.1.132 LED03_BRI Register (Address = 163h) [reset = 1FFh]

LED03_BRI is shown in Figure 159 and described in Table 139.

Return to Summary Table.

Figure 159. LED03_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led03_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led03_bri							
R/W-1FFh							

Table 139. LED03_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led03_bri	R/W	1FFh	PWM Brightness of LED03

7.6.1.133 LED04_BRI Register (Address = 164h) [reset = 1FFh]

LED04_BRI is shown in Figure 160 and described in Table 140.

Return to Summary Table.

Figure 160. LED04_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led04_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led04_bri							
R/W-1FFh							

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Table 140. LED04_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led04_bri	R/W	1FFh	PWM Brightness of LED04

7.6.1.134 LED05_BRI Register (Address = 165h) [reset = 1FFh]

LED05_BRI is shown in Figure 161 and described in Table 141.

Return to Summary Table.

Figure 161. LED05_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led05_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led05_bri							
R/W-1FFh							

Table 141. LED05_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led05_bri	R/W	1FFh	PWM Brightness of LED05

7.6.1.135 LED06_BRI Register (Address = 166h) [reset = 1FFh]

LED06_BRI is shown in Figure 162 and described in Table 142.

Return to Summary Table.

Figure 162. LED06_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led06_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led06_bri							
R/W-1FFh							

Table 142. LED06_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led06_bri	R/W	1FFh	PWM Brightness of LED06

7.6.1.136 LED07_BRI Register (Address = 167h) [reset = 1FFh]

LED07_BRI is shown in Figure 163 and described in Table 143.

Return to Summary Table.

Figure 163. LED07_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led07_bri
R/W-0h							R/W-1FFh

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7	6	5	4	3	2	1	0
led07_bri							
R/W-1FFh							

Table 143. LED07_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led07_bri	R/W	1FFh	PWM Brightness of LED07

7.6.1.137 LED08_BRI Register (Address = 168h) [reset = 1FFh]

LED08_BRI is shown in Figure 164 and described in Table 144.

Return to Summary Table.

Figure 164. LED08_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led08_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led08_bri							
R/W-1FFh							

Table 144. LED08_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led08_bri	R/W	1FFh	PWM Brightness of LED08

7.6.1.138 LED09_BRI Register (Address = 169h) [reset = 1FFh]

LED09_BRI is shown in Figure 165 and described in Table 145.

Return to Summary Table.

Figure 165. LED09_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led09_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led09_bri							
R/W-1FFh							

Table 145. LED09_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led09_bri	R/W	1FFh	PWM Brightness of LED09

7.6.1.139 LED10_BRI Register (Address = 16Ah) [reset = 1FFh]

LED10_BRI is shown in Figure 166 and described in Table 146.

Return to Summary Table.

Figure 166. LED10_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led10_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led10_bri							
R/W-1FFh							

Table 146. LED10_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led10_bri	R/W	1FFh	PWM Brightness of LED10

7.6.1.140 LED11_BRI Register (Address = 16Bh) [reset = 1FFh]

LED11_BRI is shown in Figure 167 and described in Table 147.

Return to Summary Table.

Figure 167. LED11_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led11_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led11_bri							
R/W-1FFh							

Table 147. LED11_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led11_bri	R/W	1FFh	PWM Brightness of LED11

7.6.1.141 LED12_BRI Register (Address = 16Ch) [reset = 1FFh]

LED12_BRI is shown in Figure 168 and described in Table 148.

Return to Summary Table.

Figure 168. LED12_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led12_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led12_bri							
R/W-1FFh							

Table 148. LED12_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led12_bri	R/W	1FFh	PWM Brightness of LED12

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7.6.1.142 LED13_BRI Register (Address = 16Dh) [reset = 1FFh]

LED13_BRI is shown in Figure 169 and described in Table 149.

Return to Summary Table.

Figure 169. LED13_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led13_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led13_bri							
R/W-1FFh							

Table 149. LED13_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led13_bri	R/W	1FFh	PWM Brightness of LED13

7.6.1.143 LED14_BRI Register (Address = 16Eh) [reset = 1FFh]

LED14_BRI is shown in Figure 170 and described in Table 150.

Return to Summary Table.

Figure 170. LED14_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led14_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led14_bri							
R/W-1FFh							

Table 150. LED14_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led14_bri	R/W	1FFh	PWM Brightness of LED14

7.6.1.144 LED15_BRI Register (Address = 16Fh) [reset = 1FFh]

LED15_BRI is shown in Figure 171 and described in Table 151.

Return to Summary Table.

Figure 171. LED15_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led15_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led15_bri							
R/W-1FFh							

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Table 151. LED15_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led15_bri	R/W	1FFh	PWM Brightness of LED15

7.6.1.145 LED16_BRI Register (Address = 170h) [reset = 1FFh]

LED16_BRI is shown in Figure 172 and described in Table 152.

Return to Summary Table.

Figure 172. LED16_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led16_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led16_bri							
R/W-1FFh							

Table 152. LED16_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led16_bri	R/W	1FFh	PWM Brightness of LED16

7.6.1.146 LED17_BRI Register (Address = 171h) [reset = 1FFh]

LED17_BRI is shown in Figure 173 and described in Table 153.

Return to Summary Table.

Figure 173. LED17_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led17_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led17_bri							
R/W-1FFh							

Table 153. LED17_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led17_bri	R/W	1FFh	PWM Brightness of LED17

7.6.1.147 LED18_BRI Register (Address = 172h) [reset = 1FFh]

LED18_BRI is shown in Figure 174 and described in Table 154.

Return to Summary Table.

Figure 174. LED18_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led18_bri
R/W-0h							R/W-1FFh

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7	6	5	4	3	2	1	0
led18_bri							
R/W-1FFh							

Table 154. LED18_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led18_bri	R/W	1FFh	PWM Brightness of LED18

7.6.1.148 LED19_BRI Register (Address = 173h) [reset = 1FFh]

LED19_BRI is shown in Figure 175 and described in Table 155.

Return to Summary Table.

Figure 175. LED19_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led19_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led19_bri							
R/W-1FFh							

Table 155. LED19_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led19_bri	R/W	1FFh	PWM Brightness of LED19

7.6.1.149 LED20_BRI Register (Address = 174h) [reset = 1FFh]

LED20_BRI is shown in Figure 176 and described in Table 156.

Return to Summary Table.

Figure 176. LED20_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led20_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led20_bri							
R/W-1FFh							

Table 156. LED20_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led20_bri	R/W	1FFh	PWM Brightness of LED20

7.6.1.150 LED21_BRI Register (Address = 175h) [reset = 1FFh]

LED21_BRI is shown in Figure 177 and described in Table 157.

Return to Summary Table.

Figure 177. LED21_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led21_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led21_bri							
R/W-1FFh							

Table 157. LED21_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led21_bri	R/W	1FFh	PWM Brightness of LED21

7.6.1.151 LED22_BRI Register (Address = 176h) [reset = 1FFh]

LED22_BRI is shown in Figure 178 and described in Table 158.

Return to Summary Table.

Figure 178. LED22_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led22_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led22_bri							
R/W-1FFh							

Table 158. LED22_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led22_bri	R/W	1FFh	PWM Brightness of LED22

7.6.1.152 LED23_BRI Register (Address = 177h) [reset = 1FFh]

LED23_BRI is shown in Figure 179 and described in Table 159.

Return to Summary Table.

Figure 179. LED23_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led23_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led23_bri							
R/W-1FFh							

Table 159. LED23_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led23_bri	R/W	1FFh	PWM Brightness of LED23

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7.6.1.153 LED24_BRI Register (Address = 178h) [reset = 1FFh]

LED24_BRI is shown in Figure 180 and described in Table 160.

Return to Summary Table.

Figure 180. LED24_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led24_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led24_bri							
R/W-1FFh							

Table 160. LED24_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led24_bri	R/W	1FFh	PWM Brightness of LED24

7.6.1.154 LED25_BRI Register (Address = 179h) [reset = 1FFh]

LED25_BRI is shown in Figure 181 and described in Table 161.

Return to Summary Table.

Figure 181. LED25_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led25_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led25_bri							
R/W-1FFh							

Table 161. LED25_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led25_bri	R/W	1FFh	PWM Brightness of LED25

7.6.1.155 LED26_BRI Register (Address = 17Ah) [reset = 1FFh]

LED26_BRI is shown in Figure 182 and described in Table 162.

Return to Summary Table.

Figure 182. LED26_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led26_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led26_bri							
R/W-1FFh							

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Table 162. LED26_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led26_bri	R/W	1FFh	PWM Brightness of LED26

7.6.1.156 LED27_BRI Register (Address = 17Bh) [reset = 1FFh]

LED27_BRI is shown in Figure 183 and described in Table 163.

Return to Summary Table.

Figure 183. LED27_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led27_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led27_bri							
R/W-1FFh							

Table 163. LED27_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led27_bri	R/W	1FFh	PWM Brightness of LED27

7.6.1.157 LED28_BRI Register (Address = 17Ch) [reset = 1FFh]

LED28_BRI is shown in Figure 184 and described in Table 164.

Return to Summary Table.

Figure 184. LED28_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led28_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led28_bri							
R/W-1FFh							

Table 164. LED28_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led28_bri	R/W	1FFh	PWM Brightness of LED28

7.6.1.158 LED29_BRI Register (Address = 17Dh) [reset = 1FFh]

LED29_BRI is shown in Figure 185 and described in Table 165.

Return to Summary Table.

Figure 185. LED29_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led29_bri
R/W-0h							R/W-1FFh

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7	6	5	4	3	2	1	0
led29_bri							
R/W-1FFh							

Table 165. LED29_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led29_bri	R/W	1FFh	PWM Brightness of LED29

7.6.1.159 LED30_BRI Register (Address = 17Eh) [reset = 1FFh]

LED30_BRI is shown in Figure 186 and described in Table 166.

Return to Summary Table.

Figure 186. LED30_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led30_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led30_bri							
R/W-1FFh							

Table 166. LED30_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led30_bri	R/W	1FFh	PWM Brightness of LED30

7.6.1.160 LED31_BRI Register (Address = 17Fh) [reset = 1FFh]

LED31_BRI is shown in Figure 187 and described in Table 167.

Return to Summary Table.

Figure 187. LED31_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led31_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led31_bri							
R/W-1FFh							

Table 167. LED31_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led31_bri	R/W	1FFh	PWM Brightness of LED31

7.6.1.161 LED32_BRI Register (Address = 180h) [reset = 1FFh]

LED32_BRI is shown in Figure 188 and described in Table 168.

Return to Summary Table.

Figure 188. LED32_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led32_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led32_bri							
R/W-1FFh							

Table 168. LED32_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led32_bri	R/W	1FFh	PWM Brightness of LED32

7.6.1.162 LED33_BRI Register (Address = 181h) [reset = 1FFh]

LED33_BRI is shown in Figure 189 and described in Table 169.

Return to Summary Table.

Figure 189. LED33_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led33_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led33_bri							
R/W-1FFh							

Table 169. LED33_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led33_bri	R/W	1FFh	PWM Brightness of LED33

7.6.1.163 LED34_BRI Register (Address = 182h) [reset = 1FFh]

LED34_BRI is shown in Figure 190 and described in Table 170.

Return to Summary Table.

Figure 190. LED34_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led34_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led34_bri							
R/W-1FFh							

Table 170. LED34_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led34_bri	R/W	1FFh	PWM Brightness of LED34

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7.6.1.164 LED35_BRI Register (Address = 183h) [reset = 1FFh]

LED35_BRI is shown in Figure 191 and described in Table 171.

Return to Summary Table.

Figure 191. LED35_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led35_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led35_bri							
R/W-1FFh							

Table 171. LED35_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led35_bri	R/W	1FFh	PWM Brightness of LED35

7.6.1.165 LED36_BRI Register (Address = 184h) [reset = 1FFh]

LED36_BRI is shown in Figure 192 and described in Table 172.

Return to Summary Table.

Figure 192. LED36_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led36_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led36_bri							
R/W-1FFh							

Table 172. LED36_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led36_bri	R/W	1FFh	PWM Brightness of LED36

7.6.1.166 LED37_BRI Register (Address = 185h) [reset = 1FFh]

LED37_BRI is shown in Figure 193 and described in Table 173.

Return to Summary Table.

Figure 193. LED37_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led37_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led37_bri							
R/W-1FFh							

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Table 173. LED37_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led37_bri	R/W	1FFh	PWM Brightness of LED37

7.6.1.167 LED38_BRI Register (Address = 186h) [reset = 1FFh]

LED38_BRI is shown in Figure 194 and described in Table 174.

Return to Summary Table.

Figure 194. LED38_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led38_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led38_bri							
R/W-1FFh							

Table 174. LED38_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led38_bri	R/W	1FFh	PWM Brightness of LED38

7.6.1.168 LED39_BRI Register (Address = 187h) [reset = 1FFh]

LED39_BRI is shown in Figure 195 and described in Table 175.

Return to Summary Table.

Figure 195. LED39_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led39_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led39_bri							
R/W-1FFh							

Table 175. LED39_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led39_bri	R/W	1FFh	PWM Brightness of LED39

7.6.1.169 LED40_BRI Register (Address = 188h) [reset = 1FFh]

LED40_BRI is shown in Figure 196 and described in Table 176.

Return to Summary Table.

Figure 196. LED40_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led40_bri
R/W-0h							R/W-1FFh

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7	6	5	4	3	2	1	0
led40_bri							
R/W-1FFh							

Table 176. LED40_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led40_bri	R/W	1FFh	PWM Brightness of LED40

7.6.1.170 LED41_BRI Register (Address = 189h) [reset = 1FFh]

LED41_BRI is shown in Figure 197 and described in Table 177.

Return to Summary Table.

Figure 197. LED41_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led41_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led41_bri							
R/W-1FFh							

Table 177. LED41_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led41_bri	R/W	1FFh	PWM Brightness of LED41

7.6.1.171 LED42_BRI Register (Address = 18Ah) [reset = 1FFh]

LED42_BRI is shown in Figure 198 and described in Table 178.

Return to Summary Table.

Figure 198. LED42_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led42_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led42_bri							
R/W-1FFh							

Table 178. LED42_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led42_bri	R/W	1FFh	PWM Brightness of LED42

7.6.1.172 LED43_BRI Register (Address = 18Bh) [reset = 1FFh]

LED43_BRI is shown in Figure 199 and described in Table 179.

Return to Summary Table.

Figure 199. LED43_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led43_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led43_bri							
R/W-1FFh							

Table 179. LED43_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led43_bri	R/W	1FFh	PWM Brightness of LED43

7.6.1.173 LED44_BRI Register (Address = 18Ch) [reset = 1FFh]

LED44_BRI is shown in Figure 200 and described in Table 180.

Return to Summary Table.

Figure 200. LED44_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led44_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led44_bri							
R/W-1FFh							

Table 180. LED44_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led44_bri	R/W	1FFh	PWM Brightness of LED44

7.6.1.174 LED45_BRI Register (Address = 18Dh) [reset = 1FFh]

LED45_BRI is shown in Figure 201 and described in Table 181.

Return to Summary Table.

Figure 201. LED45_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led45_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led45_bri							
R/W-1FFh							

Table 181. LED45_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led45_bri	R/W	1FFh	PWM Brightness of LED45

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7.6.1.175 LED46_BRI Register (Address = 18Eh) [reset = 1FFh]

LED46_BRI is shown in Figure 202 and described in Table 182.

Return to Summary Table.

Figure 202. LED46_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led46_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led46_bri							
R/W-1FFh							

Table 182. LED46_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led46_bri	R/W	1FFh	PWM Brightness of LED46

7.6.1.176 LED47_BRI Register (Address = 18Fh) [reset = 1FFh]

LED47_BRI is shown in Figure 203 and described in Table 183.

Return to Summary Table.

Figure 203. LED47_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led47_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led47_bri							
R/W-1FFh							

Table 183. LED47_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led47_bri	R/W	1FFh	PWM Brightness of LED47

7.6.1.177 LED48_BRI Register (Address = 190h) [reset = 1FFh]

LED48_BRI is shown in Figure 204 and described in Table 184.

Return to Summary Table.

Figure 204. LED48_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led48_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led48_bri							
R/W-1FFh							

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Table 184. LED48_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led48_bri	R/W	1FFh	PWM Brightness of LED48

7.6.1.178 LED49_BRI Register (Address = 191h) [reset = 1FFh]

LED49_BRI is shown in Figure 205 and described in Table 185.

Return to Summary Table.

Figure 205. LED49_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led49_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led49_bri							
R/W-1FFh							

Table 185. LED49_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led49_bri	R/W	1FFh	PWM Brightness of LED49

7.6.1.179 LED50_BRI Register (Address = 192h) [reset = 1FFh]

LED50_BRI is shown in Figure 206 and described in Table 186.

Return to Summary Table.

Figure 206. LED50_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led50_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led50_bri							
R/W-1FFh							

Table 186. LED50_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led50_bri	R/W	1FFh	PWM Brightness of LED50

7.6.1.180 LED51_BRI Register (Address = 193h) [reset = 1FFh]

LED51_BRI is shown in Figure 207 and described in Table 187.

Return to Summary Table.

Figure 207. LED51_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led51_bri
R/W-0h							R/W-1FFh

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7	6	5	4	3	2	1	0
led51_bri							
R/W-1FFh							

Table 187. LED51_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led51_bri	R/W	1FFh	PWM Brightness of LED51

7.6.1.181 LED52_BRI Register (Address = 194h) [reset = 1FFh]

LED52_BRI is shown in Figure 208 and described in Table 188.

Return to Summary Table.

Figure 208. LED52_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led52_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led52_bri							
R/W-1FFh							

Table 188. LED52_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led52_bri	R/W	1FFh	PWM Brightness of LED52

7.6.1.182 LED53_BRI Register (Address = 195h) [reset = 1FFh]

LED53_BRI is shown in Figure 209 and described in Table 189.

Return to Summary Table.

Figure 209. LED53_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led53_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led53_bri							
R/W-1FFh							

Table 189. LED53_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led53_bri	R/W	1FFh	PWM Brightness of LED53

7.6.1.183 LED54_BRI Register (Address = 196h) [reset = 1FFh]

LED54_BRI is shown in Figure 210 and described in Table 190.

Return to Summary Table.

Figure 210. LED54_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led54_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led54_bri							
R/W-1FFh							

Table 190. LED54_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led54_bri	R/W	1FFh	PWM Brightness of LED54

7.6.1.184 LED55_BRI Register (Address = 197h) [reset = 1FFh]

LED55_BRI is shown in Figure 211 and described in Table 191.

Return to Summary Table.

Figure 211. LED55_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led55_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led55_bri							
R/W-1FFh							

Table 191. LED55_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led55_bri	R/W	1FFh	PWM Brightness of LED55

7.6.1.185 LED56_BRI Register (Address = 198h) [reset = 1FFh]

LED56_BRI is shown in Figure 212 and described in Table 192.

Return to Summary Table.

Figure 212. LED56_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led56_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led56_bri							
R/W-1FFh							

Table 192. LED56_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led56_bri	R/W	1FFh	PWM Brightness of LED56

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7.6.1.186 LED57_BRI Register (Address = 199h) [reset = 1FFh]

LED57_BRI is shown in Figure 213 and described in Table 193.

Return to Summary Table.

Figure 213. LED57_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led57_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led57_bri							
R/W-1FFh							

Table 193. LED57_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led57_bri	R/W	1FFh	PWM Brightness of LED57

7.6.1.187 LED58_BRI Register (Address = 19Ah) [reset = 1FFh]

LED58_BRI is shown in Figure 214 and described in Table 194.

Return to Summary Table.

Figure 214. LED58_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led58_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led58_bri							
R/W-1FFh							

Table 194. LED58_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led58_bri	R/W	1FFh	PWM Brightness of LED58

7.6.1.188 LED59_BRI Register (Address = 19Bh) [reset = 1FFh]

LED59_BRI is shown in Figure 215 and described in Table 195.

Return to Summary Table.

Figure 215. LED59_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led59_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led59_bri							
R/W-1FFh							

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Table 195. LED59_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led59_bri	R/W	1FFh	PWM Brightness of LED59

7.6.1.189 LED60_BRI Register (Address = 19Ch) [reset = 1FFh]

LED60_BRI is shown in Figure 216 and described in Table 196.

Return to Summary Table.

Figure 216. LED60_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led60_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led60_bri							
R/W-1FFh							

Table 196. LED60_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led60_bri	R/W	1FFh	PWM Brightness of LED60

7.6.1.190 LED61_BRI Register (Address = 19Dh) [reset = 1FFh]

LED61_BRI is shown in Figure 217 and described in Table 197.

Return to Summary Table.

Figure 217. LED61_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led61_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led61_bri							
R/W-1FFh							

Table 197. LED61_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led61_bri	R/W	1FFh	PWM Brightness of LED61

7.6.1.191 LED62_BRI Register (Address = 19Eh) [reset = 1FFh]

LED62_BRI is shown in Figure 218 and described in Table 198.

Return to Summary Table.

Figure 218. LED62_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led62_bri
R/W-0h							R/W-1FFh

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7	6	5	4	3	2	1	0
led62_bri							
R/W-1FFh							

Table 198. LED62_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led62_bri	R/W	1FFh	PWM Brightness of LED62

7.6.1.192 LED63_BRI Register (Address = 19Fh) [reset = 1FFh]

LED63_BRI is shown in Figure 219 and described in Table 199.

Return to Summary Table.

Figure 219. LED63_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led63_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led63_bri							
R/W-1FFh							

Table 199. LED63_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led63_bri	R/W	1FFh	PWM Brightness of LED63

7.6.1.193 LED64_BRI Register (Address = 1A0h) [reset = 1FFh]

LED64_BRI is shown in Figure 220 and described in Table 200.

Return to Summary Table.

Figure 220. LED64_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led64_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led64_bri							
R/W-1FFh							

Table 200. LED64_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led64_bri	R/W	1FFh	PWM Brightness of LED64

7.6.1.194 LED65_BRI Register (Address = 1A1h) [reset = 1FFh]

LED65_BRI is shown in Figure 221 and described in Table 201.

Return to Summary Table.

Figure 221. LED65_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led65_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led65_bri							
R/W-1FFh							

Table 201. LED65_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led65_bri	R/W	1FFh	PWM Brightness of LED65

7.6.1.195 LED66_BRI Register (Address = 1A2h) [reset = 1FFh]

LED66_BRI is shown in Figure 222 and described in Table 202.

Return to Summary Table.

Figure 222. LED66_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led66_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led66_bri							
R/W-1FFh							

Table 202. LED66_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led66_bri	R/W	1FFh	PWM Brightness of LED66

7.6.1.196 LED67_BRI Register (Address = 1A3h) [reset = 1FFh]

LED67_BRI is shown in Figure 223 and described in Table 203.

Return to Summary Table.

Figure 223. LED67_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led67_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led67_bri							
R/W-1FFh							

Table 203. LED67_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led67_bri	R/W	1FFh	PWM Brightness of LED67

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7.6.1.197 LED68_BRI Register (Address = 1A4h) [reset = 1FFh]

LED68_BRI is shown in Figure 224 and described in Table 204.

Return to Summary Table.

Figure 224. LED68_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led68_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led68_bri							
R/W-1FFh							

Table 204. LED68_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led68_bri	R/W	1FFh	PWM Brightness of LED68

7.6.1.198 LED69_BRI Register (Address = 1A5h) [reset = 1FFh]

LED69_BRI is shown in Figure 225 and described in Table 205.

Return to Summary Table.

Figure 225. LED69_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led69_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led69_bri							
R/W-1FFh							

Table 205. LED69_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led69_bri	R/W	1FFh	PWM Brightness of LED69

7.6.1.199 LED70_BRI Register (Address = 1A6h) [reset = 1FFh]

LED70_BRI is shown in Figure 226 and described in Table 206.

Return to Summary Table.

Figure 226. LED70_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led70_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led70_bri							
R/W-1FFh							

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Table 206. LED70_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led70_bri	R/W	1FFh	PWM Brightness of LED70

7.6.1.200 LED71_BRI Register (Address = 1A7h) [reset = 1FFh]

LED71_BRI is shown in Figure 227 and described in Table 207.

Return to Summary Table.

Figure 227. LED71_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led71_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led71_bri							
R/W-1FFh							

Table 207. LED71_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led71_bri	R/W	1FFh	PWM Brightness of LED71

7.6.1.201 LED72_BRI Register (Address = 1A8h) [reset = 1FFh]

LED72_BRI is shown in Figure 228 and described in Table 208.

Return to Summary Table.

Figure 228. LED72_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led72_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led72_bri							
R/W-1FFh							

Table 208. LED72_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led72_bri	R/W	1FFh	PWM Brightness of LED72

7.6.1.202 LED73_BRI Register (Address = 1A9h) [reset = 1FFh]

LED73_BRI is shown in Figure 229 and described in Table 209.

Return to Summary Table.

Figure 229. LED73_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led73_bri
R/W-0h							R/W-1FFh

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7	6	5	4	3	2	1	0
led73_bri							
R/W-1FFh							

Table 209. LED73_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led73_bri	R/W	1FFh	PWM Brightness of LED73

7.6.1.203 LED74_BRI Register (Address = 1AAh) [reset = 1FFh]

LED74_BRI is shown in Figure 230 and described in Table 210.

Return to Summary Table.

Figure 230. LED74_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led74_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led74_bri							
R/W-1FFh							

Table 210. LED74_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led74_bri	R/W	1FFh	PWM Brightness of LED74

7.6.1.204 LED75_BRI Register (Address = 1ABh) [reset = 1FFh]

LED75_BRI is shown in Figure 231 and described in Table 211.

Return to Summary Table.

Figure 231. LED75_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led75_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led75_bri							
R/W-1FFh							

Table 211. LED75_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led75_bri	R/W	1FFh	PWM Brightness of LED75

7.6.1.205 LED76_BRI Register (Address = 1ACh) [reset = 1FFh]

LED76_BRI is shown in Figure 232 and described in Table 212.

Return to Summary Table.

Figure 232. LED76_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led76_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led76_bri							
R/W-1FFh							

Table 212. LED76_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led76_bri	R/W	1FFh	PWM Brightness of LED76

7.6.1.206 LED77_BRI Register (Address = 1ADh) [reset = 1FFh]

LED77_BRI is shown in Figure 233 and described in Table 213.

Return to Summary Table.

Figure 233. LED77_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led77_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led77_bri							
R/W-1FFh							

Table 213. LED77_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led77_bri	R/W	1FFh	PWM Brightness of LED77

7.6.1.207 LED78_BRI Register (Address = 1AEh) [reset = 1FFh]

LED78_BRI is shown in Figure 234 and described in Table 214.

Return to Summary Table.

Figure 234. LED78_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led78_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led78_bri							
R/W-1FFh							

Table 214. LED78_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led78_bri	R/W	1FFh	PWM Brightness of LED78

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7.6.1.208 LED79_BRI Register (Address = 1AFh) [reset = 1FFh]

LED79_BRI is shown in Figure 235 and described in Table 215.

Return to Summary Table.

Figure 235. LED79_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led79_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led79_bri							
R/W-1FFh							

Table 215. LED79_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led79_bri	R/W	1FFh	PWM Brightness of LED79

7.6.1.209 LED80_BRI Register (Address = 1B0h) [reset = 1FFh]

LED80_BRI is shown in Figure 236 and described in Table 216.

Return to Summary Table.

Figure 236. LED80_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led80_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led80_bri							
R/W-1FFh							

Table 216. LED80_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led80_bri	R/W	1FFh	PWM Brightness of LED80

7.6.1.210 LED81_BRI Register (Address = 1B1h) [reset = 1FFh]

LED81_BRI is shown in Figure 237 and described in Table 217.

Return to Summary Table.

Figure 237. LED81_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led81_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led81_bri							
R/W-1FFh							

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Table 217. LED81_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led81_bri	R/W	1FFh	PWM Brightness of LED81

7.6.1.211 LED82_BRI Register (Address = 1B2h) [reset = 1FFh]

LED82_BRI is shown in Figure 238 and described in Table 218.

Return to Summary Table.

Figure 238. LED82_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led82_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led82_bri							
R/W-1FFh							

Table 218. LED82_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led82_bri	R/W	1FFh	PWM Brightness of LED82

7.6.1.212 LED83_BRI Register (Address = 1B3h) [reset = 1FFh]

LED83_BRI is shown in Figure 239 and described in Table 219.

Return to Summary Table.

Figure 239. LED83_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led83_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led83_bri							
R/W-1FFh							

Table 219. LED83_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led83_bri	R/W	1FFh	PWM Brightness of LED83

7.6.1.213 LED84_BRI Register (Address = 1B4h) [reset = 1FFh]

LED84_BRI is shown in Figure 240 and described in Table 220.

Return to Summary Table.

Figure 240. LED84_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led84_bri
R/W-0h							R/W-1FFh

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7	6	5	4	3	2	1	0
led84_bri							
R/W-1FFh							

Table 220. LED84_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led84_bri	R/W	1FFh	PWM Brightness of LED84

7.6.1.214 LED85_BRI Register (Address = 1B5h) [reset = 1FFh]

LED85_BRI is shown in Figure 241 and described in Table 221.

Return to Summary Table.

Figure 241. LED85_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led85_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led85_bri							
R/W-1FFh							

Table 221. LED85_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led85_bri	R/W	1FFh	PWM Brightness of LED85

7.6.1.215 LED86_BRI Register (Address = 1B6h) [reset = 1FFh]

LED86_BRI is shown in Figure 242 and described in Table 222.

Return to Summary Table.

Figure 242. LED86_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led86_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led86_bri							
R/W-1FFh							

Table 222. LED86_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led86_bri	R/W	1FFh	PWM Brightness of LED86

7.6.1.216 LED87_BRI Register (Address = 1B7h) [reset = 1FFh]

LED87_BRI is shown in Figure 243 and described in Table 223.

Return to Summary Table.

Figure 243. LED87_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led87_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led87_bri							
R/W-1FFh							

Table 223. LED87_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led87_bri	R/W	1FFh	PWM Brightness of LED87

7.6.1.217 LED88_BRI Register (Address = 1B8h) [reset = 1FFh]

LED88_BRI is shown in Figure 244 and described in Table 224.

Return to Summary Table.

Figure 244. LED88_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led88_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led88_bri							
R/W-1FFh							

Table 224. LED88_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led88_bri	R/W	1FFh	PWM Brightness of LED88

7.6.1.218 LED89_BRI Register (Address = 1B9h) [reset = 1FFh]

LED89_BRI is shown in Figure 245 and described in Table 225.

Return to Summary Table.

Figure 245. LED89_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led89_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led89_bri							
R/W-1FFh							

Table 225. LED89_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led89_bri	R/W	1FFh	PWM Brightness of LED89

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7.6.1.219 LED90_BRI Register (Address = 1BAh) [reset = 1FFh]

LED90_BRI is shown in Figure 246 and described in Table 226.

Return to Summary Table.

Figure 246. LED90_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led90_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led90_bri							
R/W-1FFh							

Table 226. LED90_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led90_bri	R/W	1FFh	PWM Brightness of LED90

7.6.1.220 LED91_BRI Register (Address = 1BBh) [reset = 1FFh]

LED91_BRI is shown in Figure 247 and described in Table 227.

Return to Summary Table.

Figure 247. LED91_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led91_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led91_bri							
R/W-1FFh							

Table 227. LED91_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led91_bri	R/W	1FFh	PWM Brightness of LED91

7.6.1.221 LED92_BRI Register (Address = 1BCh) [reset = 1FFh]

LED92_BRI is shown in Figure 248 and described in Table 228.

Return to Summary Table.

Figure 248. LED92_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led92_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led92_bri							
R/W-1FFh							

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Table 228. LED92_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led92_bri	R/W	1FFh	PWM Brightness of LED92

7.6.1.222 LED93_BRI Register (Address = 1BDh) [reset = 1FFh]

LED93_BRI is shown in Figure 249 and described in Table 229.

Return to Summary Table.

Figure 249. LED93_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led93_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led93_bri							
R/W-1FFh							

Table 229. LED93_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led93_bri	R/W	1FFh	PWM Brightness of LED93

7.6.1.223 LED94_BRI Register (Address = 1BEh) [reset = 1FFh]

LED94_BRI is shown in Figure 250 and described in Table 230.

Return to Summary Table.

Figure 250. LED94_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led94_bri
R/W-0h							R/W-1FFh
7	6	5	4	3	2	1	0
led94_bri							
R/W-1FFh							

Table 230. LED94_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led94_bri	R/W	1FFh	PWM Brightness of LED94

7.6.1.224 LED95_BRI Register (Address = 1BFh) [reset = 1FFh]

LED95_BRI is shown in Figure 251 and described in Table 231.

Return to Summary Table.

Figure 251. LED95_BRI Register

15	14	13	12	11	10	9	8
RESERVED							led95_bri
R/W-0h							R/W-1FFh

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7	6	5	4	3	2	1	0
led95_bri							
R/W-1FFh							

Table 231. LED95_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	led95_bri	R/W	1FFh	PWM Brightness of LED95

7.6.1.225 MASTER_BRI Register (Address = 1C0h) [reset = 0h]

MASTER_BRI is shown in Figure 252 and described in Table 232.

Return to Summary Table.

Figure 252. MASTER_BRI Register

15	14	13	12	11	10	9	8
RESERVED							master_bri
R/W-0h							R/W-0h
7	6	5	4	3	2	1	0
master_bri							
R/W-0h							

Table 232. MASTER_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	master_bri	R/W	0h	Master Brightness of all LEDs

7.6.1.226 LED07_00_DISABLE Register (Address = 1C1h) [reset = 0h]

LED07_00_DISABLE is shown in Figure 253 and described in Table 233.

Return to Summary Table.

Figure 253. LED07_00_DISABLE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led07_00_disable							
R/W-0h							

Table 233. LED07_00_DISABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led07_00_disable	R/W	0h	LED disable bits for LEDs 0-7: 0=Enable 1=Disable

7.6.1.227 LED15_08_DISABLE Register (Address = 1C2h) [reset = 0h]

LED15_08_DISABLE is shown in Figure 254 and described in Table 234.

Return to Summary Table.

Figure 254. LED15_08_DISABLE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led15_08_disable							
R/W-0h							

Table 234. LED15_08_DISABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led15_08_disable	R/W	0h	LED disable bits for LEDs 8-15: 0=Enable 1=Disable

7.6.1.228 LED23_16_DISABLE Register (Address = 1C3h) [reset = 0h]

LED23_16_DISABLE is shown in Figure 255 and described in Table 235.

Return to Summary Table.

Figure 255. LED23_16_DISABLE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led23_16_disable							
R/W-0h							

Table 235. LED23_16_DISABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led23_16_disable	R/W	0h	LED disable bits for LEDs 16-23: 0=Enable 1=Disable

7.6.1.229 LED31_24_DISABLE Register (Address = 1C4h) [reset = 0h]

LED31_24_DISABLE is shown in Figure 256 and described in Table 236.

Return to Summary Table.

Figure 256. LED31_24_DISABLE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led31_24_disable							
R/W-0h							

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Table 236. LED31_24_DISABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led31_24_disable	R/W	0h	LED disable bits for LEDs 24-31: 0=Enable 1=Disable

7.6.1.230 LED39_32_DISABLE Register (Address = 1C5h) [reset = 0h]

LED39_32_DISABLE is shown in Figure 257 and described in Table 237.

Return to Summary Table.

Figure 257. LED39_32_DISABLE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led39_32_disable							
R/W-0h							

Table 237. LED39_32_DISABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led39_32_disable	R/W	0h	LED disable bits for LEDs 39-32: 0=Enable 1=Disable

7.6.1.231 LED47_40_DISABLE Register (Address = 1C6h) [reset = 0h]

LED47_40_DISABLE is shown in Figure 258 and described in Table 238.

Return to Summary Table.

Figure 258. LED47_40_DISABLE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led47_40_disable							
R/W-0h							

Table 238. LED47_40_DISABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led47_40_disable	R/W	0h	LED disable bits for LEDs 40-47: 0=Enable 1=Disable

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7.6.1.232 LED55_48_DISABLE Register (Address = 1C7h) [reset = 0h]

LED55_48_DISABLE is shown in Figure 259 and described in Table 239.

Return to Summary Table.

Figure 259. LED55_48_DISABLE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led55_48_disable							
R/W-0h							

Table 239. LED55_48_DISABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led55_48_disable	R/W	0h	LED disable bits for LEDs 48-54: 0=Enable 1=Disable

7.6.1.233 LED63_56_DISABLE Register (Address = 1C8h) [reset = 0h]

LED63_56_DISABLE is shown in Figure 260 and described in Table 240.

Return to Summary Table.

Figure 260. LED63_56_DISABLE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led63_56_disable							
R/W-0h							

Table 240. LED63_56_DISABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led63_56_disable	R/W	0h	LED disable bits for LEDs 56-63: 0=Enable 1=Disable

7.6.1.234 LED71_64_DISABLE Register (Address = 1C9h) [reset = 0h]

LED71_64_DISABLE is shown in Figure 261 and described in Table 241.

Return to Summary Table.

Figure 261. LED71_64_DISABLE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led71_64_disable							
R/W-0h							

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Table 241. LED71_64_DISABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led71_64_disable	R/W	0h	LED disable bits for LEDs 64-71: 0=Enable 1=Disable

7.6.1.235 LED79_72_DISABLE Register (Address = 1CAh) [reset = 0h]

LED79_72_DISABLE is shown in Figure 262 and described in Table 242.

Return to Summary Table.

Figure 262. LED79_72_DISABLE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led79_72_disable							
R/W-0h							

Table 242. LED79_72_DISABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led79_72_disable	R/W	0h	LED disable bits for LEDs 72-79: 0=Enable 1=Disable

7.6.1.236 LED87_80_DISABLE Register (Address = 1CBh) [reset = 0h]

LED87_80_DISABLE is shown in Figure 263 and described in Table 243.

Return to Summary Table.

Figure 263. LED87_80_DISABLE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led87_80_disable							
R/W-0h							

Table 243. LED87_80_DISABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led87_80_disable	R/W	0h	LED disable bits for LEDs 80-87: 0=Enable 1=Disable

7.6.1.237 LED95_88_DISABLE Register (Address = 1CCh) [reset = 0h]

LED95_88_DISABLE is shown in Figure 264 and described in Table 244.

Return to Summary Table.

Figure 264. LED95_88_DISABLE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led95_88_disable							
R/W-0h							

Table 244. LED95_88_DISABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led95_88_disable	R/W	0h	LED disable bits for LEDs 88-95: 0=Enable 1=Disable

7.6.1.238 SLOPERS_CONFIG Register (Address = 1CDh) [reset = 15h]

SLOPERS_CONFIG is shown in Figure 265 and described in Table 245.

Return to Summary Table.

Figure 265. SLOPERS_CONFIG Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-15h							
7	6	5	4	3	2	1	0
RESERVED			matrix_slope_sel		master_slope_sel		master_slope_en
R/W-0h			R/W-2h		R/W-2h		R/W-1h

Table 245. SLOPERS_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R/W	0h	
4-3	matrix_slope_sel	R/W	2h	Timing configuration of Matrix Sloper: 00=2ms (Advanced Sloper off), 01=10ms (Advanced Sloper off), 10=50ms (Advanced Sloper on), 11=200ms (Advanced Sloper on)
2-1	master_slope_sel	R/W	2h	Timing configuration of Master Sloper: 00=2ms (Advanced Sloper off), 01=10ms (Advanced Sloper off), 10=50ms (Advanced Sloper on), 11=200ms (Advanced Sloper on)
0	master_slope_en	R/W	1h	Enable of Master Brightness Sloper

7.6.1.239 SLOPER_TARGET Register (Address = 1CEh) [reset = 0h]

SLOPER_TARGET is shown in Figure 266 and described in Table 246.

Return to Summary Table.

Figure 266. SLOPER_TARGET Register

15	14	13	12	11	10	9	8
RESERVED							sloper_target
R-0h							0h

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7	6	5	4	3	2	1	0
sloper_target							
0h							

Table 246. SLOPER_TARGET Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	
8-0	sloper_target		0h	Target brightness of Matrix Sloper

7.6.1.240 LED07_00_SLOPE Register (Address = 1CFh) [reset = 0h]

LED07_00_SLOPE is shown in Figure 267 and described in Table 247.

Return to Summary Table.

Figure 267. LED07_00_SLOPE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led07_00_slope							
R/W-0h							

Table 247. LED07_00_SLOPE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led07_00_slope	R/W	0h	Matrix Sloper selection bits for LEDs 0-7: 0=LED is not part of sloping, 1=LED is part of sloping

7.6.1.241 LED15_08_SLOPE Register (Address = 1D0h) [reset = 0h]

LED15_08_SLOPE is shown in Figure 268 and described in Table 248.

Return to Summary Table.

Figure 268. LED15_08_SLOPE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led15_08_slope							
R/W-0h							

Table 248. LED15_08_SLOPE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led15_08_slope	R/W	0h	Matrix Sloper selection bits for LEDs 8-15: 0=LED is not part of sloping, 1=LED is part of sloping

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7.6.1.242 LED23_16_SLOPE Register (Address = 1D1h) [reset = 0h]

LED23_16_SLOPE is shown in Figure 269 and described in Table 249.

Return to Summary Table.

Figure 269. LED23_16_SLOPE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led23_16_slope							
R/W-0h							

Table 249. LED23_16_SLOPE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led23_16_slope	R/W	0h	Matrix Sloper selection bits for LEDs 16-23: 0=LED is not part of sloping, 1=LED is part of sloping

7.6.1.243 LED31_24_SLOPE Register (Address = 1D2h) [reset = 0h]

LED31_24_SLOPE is shown in Figure 270 and described in Table 250.

Return to Summary Table.

Figure 270. LED31_24_SLOPE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led31_24_slope							
R/W-0h							

Table 250. LED31_24_SLOPE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led31_24_slope	R/W	0h	Matrix Sloper selection bits for LEDs 24-31: 0=LED is not part of sloping, 1=LED is part of sloping

7.6.1.244 LED39_32_SLOPE Register (Address = 1D3h) [reset = 0h]

LED39_32_SLOPE is shown in Figure 271 and described in Table 251.

Return to Summary Table.

Figure 271. LED39_32_SLOPE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led39_32_slope							
R/W-0h							

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Table 251. LED39_32_SLOPE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led39_32_slope	R/W	0h	Matrix Sloper selection bits for LEDs 32-39: 0=LED is not part of sloping, 1=LED is part of sloping

7.6.1.245 LED47_40_SLOPE Register (Address = 1D4h) [reset = 0h]

LED47_40_SLOPE is shown in Figure 272 and described in Table 252.

Return to Summary Table.

Figure 272. LED47_40_SLOPE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led47_40_slope							
R/W-0h							

Table 252. LED47_40_SLOPE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led47_40_slope	R/W	0h	Matrix Sloper selection bits for LEDs 40-47: 0=LED is not part of sloping, 1=LED is part of sloping

7.6.1.246 LED55_48_SLOPE Register (Address = 1D5h) [reset = 0h]

LED55_48_SLOPE is shown in Figure 273 and described in Table 253.

Return to Summary Table.

Figure 273. LED55_48_SLOPE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led55_48_slope							
R/W-0h							

Table 253. LED55_48_SLOPE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led55_48_slope	R/W	0h	Matrix Sloper selection bits for LEDs 48-55: 0=LED is not part of sloping, 1=LED is part of sloping

7.6.1.247 LED63_56_SLOPE Register (Address = 1D6h) [reset = 0h]

LED63_56_SLOPE is shown in Figure 274 and described in Table 254.

Return to Summary Table.

Figure 274. LED63_56_SLOPE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led63_56_slope							
R/W-0h							

Table 254. LED63_56_SLOPE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led63_56_slope	R/W	0h	Matrix Sloper selection bits for LEDs 56-63: 0=LED is not part of sloping, 1=LED is part of sloping

7.6.1.248 LED71_64_SLOPE Register (Address = 1D7h) [reset = 0h]

LED71_64_SLOPE is shown in Figure 275 and described in Table 255.

Return to Summary Table.

Figure 275. LED71_64_SLOPE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led71_64_slope							
R/W-0h							

Table 255. LED71_64_SLOPE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led71_64_slope	R/W	0h	Matrix Sloper selection bits for LEDs 64-71: 0=LED is not part of sloping, 1=LED is part of sloping

7.6.1.249 LED79_72_SLOPE Register (Address = 1D8h) [reset = 0h]

LED79_72_SLOPE is shown in Figure 276 and described in Table 256.

Return to Summary Table.

Figure 276. LED79_72_SLOPE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led79_72_slope							
R/W-0h							

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Table 256. LED79_72_SLOPE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led79_72_slope	R/W	0h	Matrix Sloper selection bits for LEDs 72-79: 0=LED is not part of sloping, 1=LED is part of sloping

7.6.1.250 LED87_80_SLOPE Register (Address = 1D9h) [reset = 0h]

LED87_80_SLOPE is shown in Figure 277 and described in Table 257.

Return to Summary Table.

Figure 277. LED87_80_SLOPE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led87_80_slope							
R/W-0h							

Table 257. LED87_80_SLOPE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led87_80_slope	R/W	0h	Matrix Sloper selection bits for LEDs 80-87: 0=LED is not part of sloping, 1=LED is part of sloping

7.6.1.251 LED95_88_SLOPE Register (Address = 1DAh) [reset = 0h]

LED95_88_SLOPE is shown in Figure 278 and described in Table 258.

Return to Summary Table.

Figure 278. LED95_88_SLOPE Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
led95_88_slope							
R/W-0h							

Table 258. LED95_88_SLOPE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	
7-0	led95_88_slope	R/W	0h	Matrix Sloper selection bits for LEDs 88-95: 0=LED is not part of sloping, 1=LED is part of sloping

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7.6.1.252 LEDGRP1_BRI Register (Address = 1DBh) [reset = 0h]

LEDGRP1_BRI is shown in Figure 279 and described in Table 259.

Return to Summary Table.

Figure 279. LEDGRP1_BRI Register

15	14	13	12	11	10	9	8
RESERVED							ledgrp1_bri
R/W-0h							R/W-0h
7	6	5	4	3	2	1	0
ledgrp1_bri							
R/W-0h							

Table 259. LEDGRP1_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	ledgrp1_bri	R/W	0h	Brightness of Group #1 LEDs

7.6.1.253 LEDGRP2_BRI Register (Address = 1DCh) [reset = 0h]

LEDGRP2_BRI is shown in Figure 280 and described in Table 260.

Return to Summary Table.

Figure 280. LEDGRP2_BRI Register

15	14	13	12	11	10	9	8
RESERVED							ledgrp2_bri
R/W-0h							R/W-0h
7	6	5	4	3	2	1	0
ledgrp2_bri							
R/W-0h							

Table 260. LEDGRP2_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	ledgrp2_bri	R/W	0h	Brightness of Group #2 LEDs

7.6.1.254 LEDGRP3_BRI Register (Address = 1DDh) [reset = 0h]

LEDGRP3_BRI is shown in Figure 281 and described in Table 261.

Return to Summary Table.

Figure 281. LEDGRP3_BRI Register

15	14	13	12	11	10	9	8
RESERVED							ledgrp3_bri
R/W-0h							R/W-0h
7	6	5	4	3	2	1	0
ledgrp3_bri							
R/W-0h							

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Table 261. LEDGRP3_BRI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	
8-0	ledgrp3_bri	R/W	0h	Brightness of Group #3 LEDs

7.6.1.255 LED04_00_GRPSEL Register (Address = 1DEh) [reset = 0h]

LED04_00_GRPSEL is shown in Figure 282 and described in Table 262.

Return to Summary Table.

Figure 282. LED04_00_GRPSEL Register

15	14	13	12	11	10	9	8
RESERVED						led04_grp	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
led03_grp		led02_grp		led01_grp		led00_grp	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 262. LED04_00_GRPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	
9-8	led04_grp	R/W	0h	Group selection for LED04: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
7-6	led03_grp	R/W	0h	Group selection for LED03: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
5-4	led02_grp	R/W	0h	Group selection for LED02: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
3-2	led01_grp	R/W	0h	Group selection for LED01: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
1-0	led00_grp	R/W	0h	Group selection for LED00: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

7.6.1.256 LED09_05_GRPSEL Register (Address = 1DFh) [reset = 0h]

LED09_05_GRPSEL is shown in Figure 283 and described in Table 263.

Return to Summary Table.

Figure 283. LED09_05_GRPSEL Register

15	14	13	12	11	10	9	8
RESERVED						led09_grp	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
led08_grp		led07_grp		led06_grp		led05_grp	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 263. LED09_05_GRPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	
9-8	led09_grp	R/W	0h	Group selection for LED09: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
7-6	led08_grp	R/W	0h	Group selection for LED08: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
5-4	led07_grp	R/W	0h	Group selection for LED07: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
3-2	led06_grp	R/W	0h	Group selection for LED06: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
1-0	led05_grp	R/W	0h	Group selection for LED05: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

7.6.1.257 LED14_10_GRPSEL Register (Address = 1E0h) [reset = 0h]

LED14_10_GRPSEL is shown in Figure 284 and described in Table 264.

Return to Summary Table.

Figure 284. LED14_10_GRPSEL Register

15	14	13	12	11	10	9	8
RESERVED						led14_grp	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
led13_grp		led12_grp		led11_grp		led10_grp	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

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Table 264. LED14_10_GRPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	
9-8	led14_grp	R/W	0h	Group selection for LED14: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
7-6	led13_grp	R/W	0h	Group selection for LED13: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
5-4	led12_grp	R/W	0h	Group selection for LED12: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
3-2	led11_grp	R/W	0h	Group selection for LED11: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
1-0	led10_grp	R/W	0h	Group selection for LED10: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

7.6.1.258 LED19_15_GRPSEL Register (Address = 1E1h) [reset = 0h]

LED19_15_GRPSEL is shown in Figure 285 and described in Table 265.

Return to Summary Table.

Figure 285. LED19_15_GRPSEL Register

15	14	13	12	11	10	9	8
RESERVED						led19_grp	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
led18_grp		led17_grp		led16_grp		led15_grp	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 265. LED19_15_GRPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	
9-8	led19_grp	R/W	0h	Group selection for LED19: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

Table 265. LED19_15_GRPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	led18_grp	R/W	0h	Group selection for LED18: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
5-4	led17_grp	R/W	0h	Group selection for LED17: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
3-2	led16_grp	R/W	0h	Group selection for LED16: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
1-0	led15_grp	R/W	0h	Group selection for LED15: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

7.6.1.259 LED24_20_GRPSEL Register (Address = 1E2h) [reset = 0h]

LED24_20_GRPSEL is shown in Figure 286 and described in Table 266.

Return to Summary Table.

Figure 286. LED24_20_GRPSEL Register

15	14	13	12	11	10	9	8
RESERVED						led24_grp	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
led23_grp		led22_grp		led21_grp		led20_grp	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 266. LED24_20_GRPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	
9-8	led24_grp	R/W	0h	Group selection for LED24: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
7-6	led23_grp	R/W	0h	Group selection for LED23: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
5-4	led22_grp	R/W	0h	Group selection for LED22: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

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Table 266. LED24_20_GRPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	led21_grp	R/W	0h	Group selection for LED21: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
1-0	led20_grp	R/W	0h	Group selection for LED20: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

7.6.1.260 LED29_25_GRPSEL Register (Address = 1E3h) [reset = 0h]

LED29_25_GRPSEL is shown in Figure 287 and described in Table 267.

Return to Summary Table.

Figure 287. LED29_25_GRPSEL Register

15	14	13	12	11	10	9	8
RESERVED						led29_grp	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
led28_grp		led27_grp		led26_grp		led25_grp	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 267. LED29_25_GRPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	
9-8	led29_grp	R/W	0h	Group selection for LED29: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
7-6	led28_grp	R/W	0h	Group selection for LED28: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
5-4	led27_grp	R/W	0h	Group selection for LED27: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
3-2	led26_grp	R/W	0h	Group selection for LED26: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
1-0	led25_grp	R/W	0h	Group selection for LED25: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

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7.6.1.261 LED34_30_GRPSEL Register (Address = 1E4h) [reset = 0h]

LED34_30_GRPSEL is shown in Figure 288 and described in Table 268.

Return to Summary Table.

Figure 288. LED34_30_GRPSEL Register

15	14	13	12	11	10	9	8
RESERVED						led34_grp	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
led33_grp		led32_grp		led31_grp		led30_grp	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 268. LED34_30_GRPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	
9-8	led34_grp	R/W	0h	Group selection for LED34: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
7-6	led33_grp	R/W	0h	Group selection for LED33: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
5-4	led32_grp	R/W	0h	Group selection for LED32: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
3-2	led31_grp	R/W	0h	Group selection for LED31: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
1-0	led30_grp	R/W	0h	Group selection for LED30: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

7.6.1.262 LED39_35_GRPSEL Register (Address = 1E5h) [reset = 0h]

LED39_35_GRPSEL is shown in Figure 289 and described in Table 269.

Return to Summary Table.

Figure 289. LED39_35_GRPSEL Register

15	14	13	12	11	10	9	8
RESERVED						led39_grp	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
led38_grp		led37_grp		led36_grp		led35_grp	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

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Table 269. LED39_35_GRPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	
9-8	led39_grp	R/W	0h	Group selection for LED39: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
7-6	led38_grp	R/W	0h	Group selection for LED38: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
5-4	led37_grp	R/W	0h	Group selection for LED37: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
3-2	led36_grp	R/W	0h	Group selection for LED36: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
1-0	led35_grp	R/W	0h	Group selection for LED35: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

7.6.1.263 LED44_40_GRPSEL Register (Address = 1E6h) [reset = 0h]

LED44_40_GRPSEL is shown in Figure 290 and described in Table 270.

Return to Summary Table.

Figure 290. LED44_40_GRPSEL Register

15	14	13	12	11	10	9	8
RESERVED						led44_grp	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
led43_grp		led42_grp		led41_grp		led40_grp	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 270. LED44_40_GRPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	
9-8	led44_grp	R/W	0h	Group selection for LED44: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
7-6	led43_grp	R/W	0h	Group selection for LED43: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

Table 270. LED44_40_GRPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	led42_grp	R/W	0h	Group selection for LED42: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
3-2	led41_grp	R/W	0h	Group selection for LED41: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
1-0	led40_grp	R/W	0h	Group selection for LED40: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

7.6.1.264 LED49_45_GRPSEL Register (Address = 1E7h) [reset = 0h]

LED49_45_GRPSEL is shown in Figure 291 and described in Table 271.

Return to Summary Table.

Figure 291. LED49_45_GRPSEL Register

15	14	13	12	11	10	9	8
RESERVED						led49_grp	
R/W-0h						R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
led48_grp		led47_grp		led46_grp		led45_grp	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 271. LED49_45_GRPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	
9-8	led49_grp	R/W	0h	Group selection for LED49: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
7-6	led48_grp	R/W	0h	Group selection for LED48: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
5-4	led47_grp	R/W	0h	Group selection for LED47: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
3-2	led46_grp	R/W	0h	Group selection for LED46: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

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Table 271. LED49_45_GRPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	led45_grp	R/W	0h	Group selection for LED45: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

7.6.1.265 LED54_50_GRPSEL Register (Address = 1E8h) [reset = 0h]

LED54_50_GRPSEL is shown in Figure 292 and described in Table 272.

Return to Summary Table.

Figure 292. LED54_50_GRPSEL Register

15	14	13	12	11	10	9	8
RESERVED						led54_grp	
R/W-0h						R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
led53_grp		led52_grp		led51_grp		led50_grp	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 272. LED54_50_GRPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	
9-8	led54_grp	R/W	0h	Group selection for LED54: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
7-6	led53_grp	R/W	0h	Group selection for LED53: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
5-4	led52_grp	R/W	0h	Group selection for LED52: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
3-2	led51_grp	R/W	0h	Group selection for LED51: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
1-0	led50_grp	R/W	0h	Group selection for LED50: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

7.6.1.266 LED59_55_GRPSEL Register (Address = 1E9h) [reset = 0h]

LED59_55_GRPSEL is shown in Figure 293 and described in Table 273.

Return to Summary Table.

Figure 293. LED59_55_GRPSEL Register

15	14	13	12	11	10	9	8
RESERVED						led59_grp	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
led58_grp		led57_grp		led56_grp		led55_grp	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 273. LED59_55_GRPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	
9-8	led59_grp	R/W	0h	Group selection for LED59: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
7-6	led58_grp	R/W	0h	Group selection for LED58: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
5-4	led57_grp	R/W	0h	Group selection for LED57: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
3-2	led56_grp	R/W	0h	Group selection for LED56: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
1-0	led55_grp	R/W	0h	Group selection for LED55: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

7.6.1.267 LED64_60_GRPSEL Register (Address = 1EAh) [reset = 0h]

LED64_60_GRPSEL is shown in Figure 294 and described in Table 274.

Return to Summary Table.

Figure 294. LED64_60_GRPSEL Register

15	14	13	12	11	10	9	8
RESERVED						led64_grp	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
led63_grp		led62_grp		led61_grp		led60_grp	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

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Table 274. LED64_60_GRPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	
9-8	led64_grp	R/W	0h	Group selection for LED64: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
7-6	led63_grp	R/W	0h	Group selection for LED63: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
5-4	led62_grp	R/W	0h	Group selection for LED62: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
3-2	led61_grp	R/W	0h	Group selection for LED61: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
1-0	led60_grp	R/W	0h	Group selection for LED60: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

7.6.1.268 LED69_65_GRPSEL Register (Address = 1EBh) [reset = 0h]

LED69_65_GRPSEL is shown in Figure 295 and described in Table 275.

Return to Summary Table.

Figure 295. LED69_65_GRPSEL Register

15	14	13	12	11	10	9	8
RESERVED						led69_grp	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
led68_grp		led67_grp		led66_grp		led65_grp	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 275. LED69_65_GRPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	
9-8	led69_grp	R/W	0h	Group selection for LED69: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

Table 275. LED69_65_GRPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	led68_grp	R/W	0h	Group selection for LED68: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
5-4	led67_grp	R/W	0h	Group selection for LED67: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
3-2	led66_grp	R/W	0h	Group selection for LED66: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
1-0	led65_grp	R/W	0h	Group selection for LED65: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

7.6.1.269 LED74_70_GRPSEL Register (Address = 1ECh) [reset = 0h]

LED74_70_GRPSEL is shown in Figure 296 and described in Table 276.

Return to Summary Table.

Figure 296. LED74_70_GRPSEL Register

15	14	13	12	11	10	9	8
RESERVED						led74_grp	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
led73_grp		led72_grp		led71_grp		led70_grp	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 276. LED74_70_GRPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	
9-8	led74_grp	R/W	0h	Group selection for LED74: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
7-6	led73_grp	R/W	0h	Group selection for LED73: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
5-4	led72_grp	R/W	0h	Group selection for LED72: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

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Table 276. LED74_70_GRPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	led71_grp	R/W	0h	Group selection for LED71: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
1-0	led70_grp	R/W	0h	Group selection for LED70: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

7.6.1.270 LED79_75_GRPSEL Register (Address = 1EDh) [reset = 0h]

LED79_75_GRPSEL is shown in Figure 297 and described in Table 277.

Return to Summary Table.

Figure 297. LED79_75_GRPSEL Register

15	14	13	12	11	10	9	8
RESERVED						led79_grp	
R/W-0h						R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
led78_grp		led77_grp		led76_grp		led75_grp	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 277. LED79_75_GRPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	
9-8	led79_grp	R/W	0h	Group selection for LED79: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
7-6	led78_grp	R/W	0h	Group selection for LED78: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
5-4	led77_grp	R/W	0h	Group selection for LED77: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
3-2	led76_grp	R/W	0h	Group selection for LED76: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
1-0	led75_grp	R/W	0h	Group selection for LED75: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

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7.6.1.271 LED84_80_GRPSEL Register (Address = 1EEh) [reset = 0h]

LED84_80_GRPSEL is shown in Figure 298 and described in Table 278.

Return to Summary Table.

Figure 298. LED84_80_GRPSEL Register

15	14	13	12	11	10	9	8
RESERVED						led84_grp	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
led83_grp		led82_grp		led81_grp		led80_grp	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 278. LED84_80_GRPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	
9-8	led84_grp	R/W	0h	Group selection for LED84: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
7-6	led83_grp	R/W	0h	Group selection for LED83: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
5-4	led82_grp	R/W	0h	Group selection for LED82: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
3-2	led81_grp	R/W	0h	Group selection for LED81: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
1-0	led80_grp	R/W	0h	Group selection for LED80: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

7.6.1.272 LED89_85_GRPSEL Register (Address = 1EFh) [reset = 0h]

LED89_85_GRPSEL is shown in Figure 299 and described in Table 279.

Return to Summary Table.

Figure 299. LED89_85_GRPSEL Register

15	14	13	12	11	10	9	8
RESERVED						led89_grp	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
led88_grp		led87_grp		led86_grp		led85_grp	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

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Table 279. LED89_85_GRPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	
9-8	led89_grp	R/W	0h	Group selection for LED89: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
7-6	led88_grp	R/W	0h	Group selection for LED88: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
5-4	led87_grp	R/W	0h	Group selection for LED87: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
3-2	led86_grp	R/W	0h	Group selection for LED86: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
1-0	led85_grp	R/W	0h	Group selection for LED85: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

7.6.1.273 LED94_90_GRPSEL Register (Address = 1F0h) [reset = 0h]

LED94_90_GRPSEL is shown in Figure 300 and described in Table 280.

Return to Summary Table.

Figure 300. LED94_90_GRPSEL Register

15	14	13	12	11	10	9	8
RESERVED						led94_grp	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
led93_grp		led92_grp		led91_grp		led90_grp	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 280. LED94_90_GRPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	
9-8	led94_grp	R/W	0h	Group selection for LED94: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
7-6	led93_grp	R/W	0h	Group selection for LED93: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

Table 280. LED94_90_GRPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	led92_grp	R/W	0h	Group selection for LED92: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
3-2	led91_grp	R/W	0h	Group selection for LED91: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3
1-0	led90_grp	R/W	0h	Group selection for LED90: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

7.6.1.274 LED95_GRPSEL Register (Address = 1F1h) [reset = 0h]

LED95_GRPSEL is shown in Figure 301 and described in Table 281.

Return to Summary Table.

Figure 301. LED95_GRPSEL Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						led95_grp	
R/W-0h						R/W-0h	

Table 281. LED95_GRPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R/W	0h	
1-0	led95_grp	R/W	0h	Group selection for LED95: 00=No member of grouping, 01=Member of Group #1, 10=Member of Group #2, 11=Member of Group #3

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LED171596A is an LED driver that can individually control up to 96 LEDs. The maximum LED current for all LED driver outputs is configured by the value of RISET resistor and LEDXX_CUR[7:0] registers. Refer to Table 283 for RISET current calculation.

8.2 Typical Application

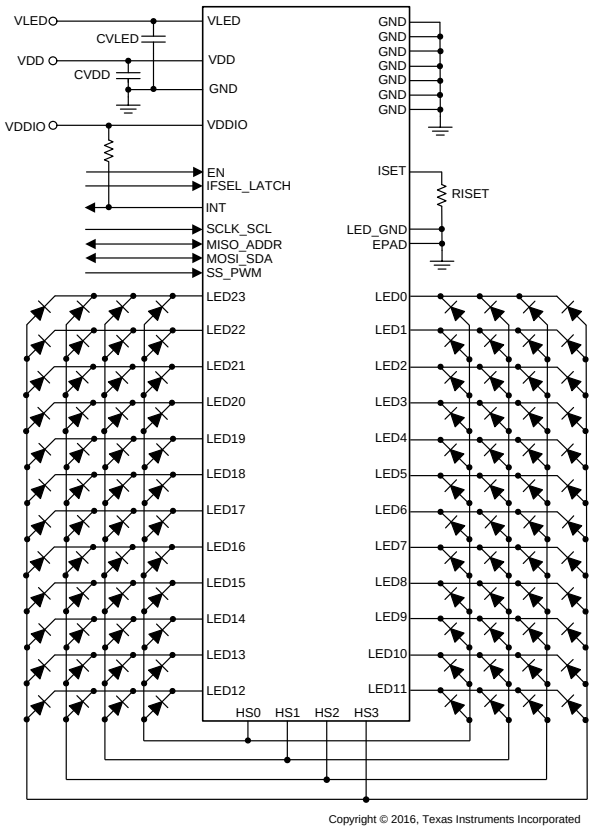

Figure 302. Typical Application

Typical Application (continued)

8.2.1 Design Requirements

The following design guideline provides a component selection to operate the device within the recommended operating conditions.

Table 282. List of Components

REFERENCE	DESCRIPTION	PART NUMBER	MANUFACTURER
IC	96-Channel LED Driver, QFN	LED171596A	Texas Instruments
CVLED	CAP, CERM, 10 µF, 10 V	C0805C106K8RACTU	Kemet
CVDD	CAP, CERM, 10 µF, 6.3 V	C1608JB0J106K080AB	TDK
RISET	RES, 12.4k, 1%, 0.1 W, 0603	CRCW060312K4FKEA	Vishay-Dale

8.2.2 Detailed Design Procedure

The default value of LEDXX_CUR[7:0] registers is 0xCC or 80% of peak current. Using this value the required RISET value for 2.48 mA average LED current is shown in Table 283.

Table 283. RISET Example Calculation

ISET (mA)	RISET CALCULATED (kΩ)	RISET STANDARD VALUE (kΩ)	LEDXX_CUR	PEAK ILED CURRENT (mA)	AVERAGE ILED CURRENT (mA)
10	60	60.4	0xCC	9.93	2.48

8.2.3 Application Curves

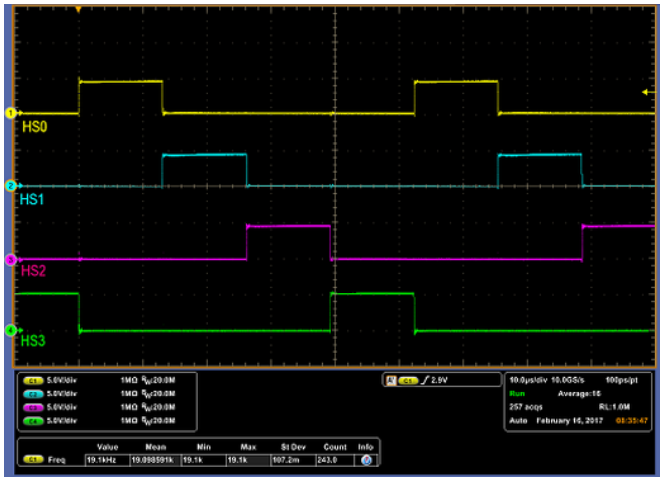

Figure 303. High Side Switch Sequence

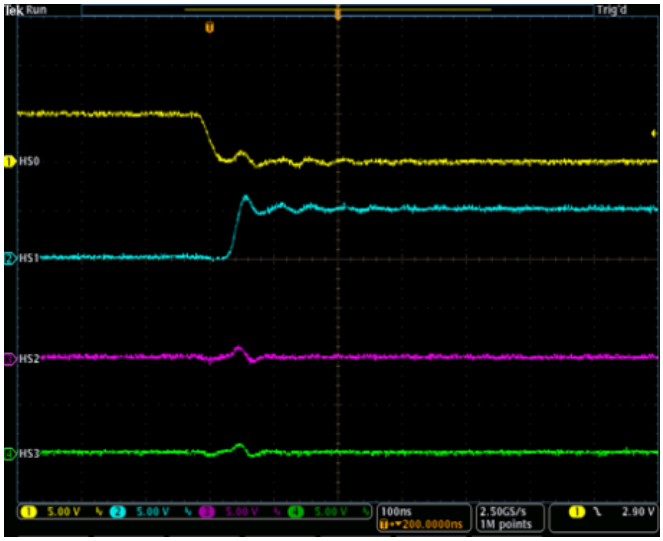

Figure 304. HS0 to HS1 Transition

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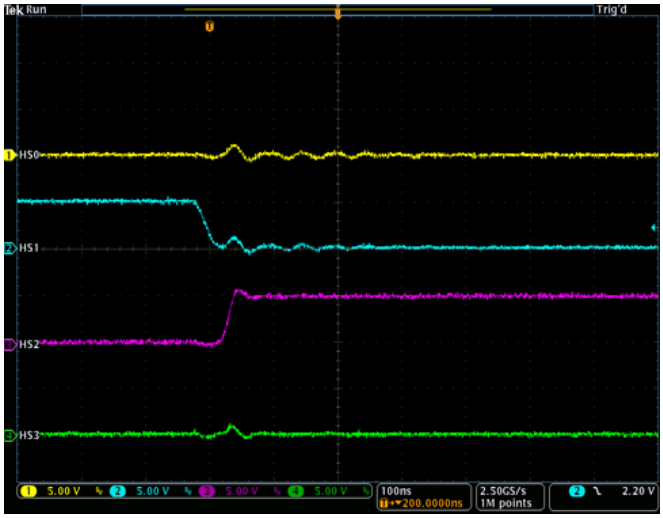

Figure 305. HS1 to HS2 Transition

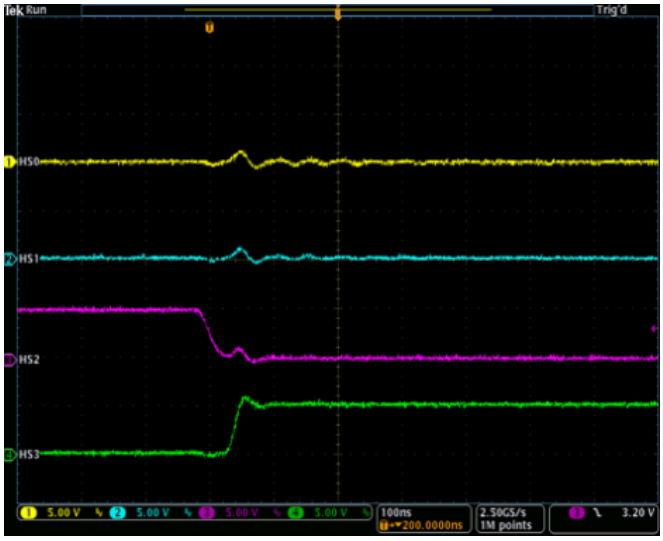

Figure 306. HS2 to HS3 Transition

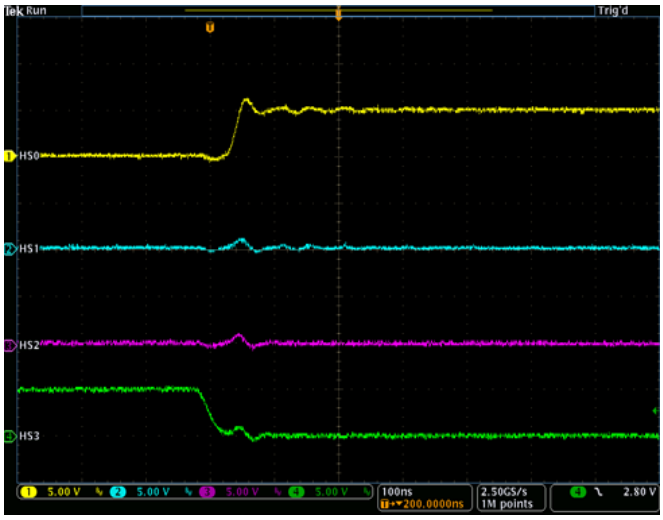

Figure 307. HS3 to HS0 Transition

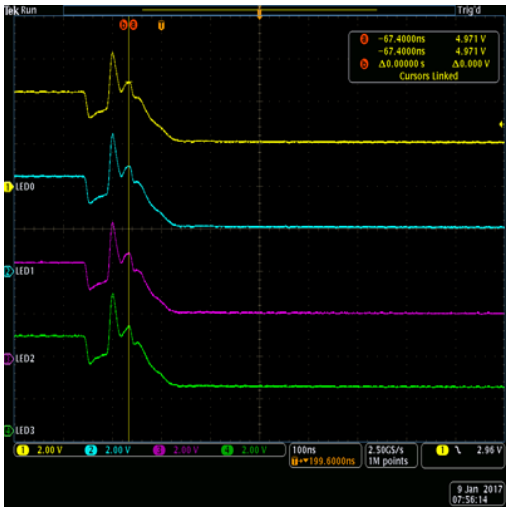

Figure 308. LED PWM Phase Shift 0

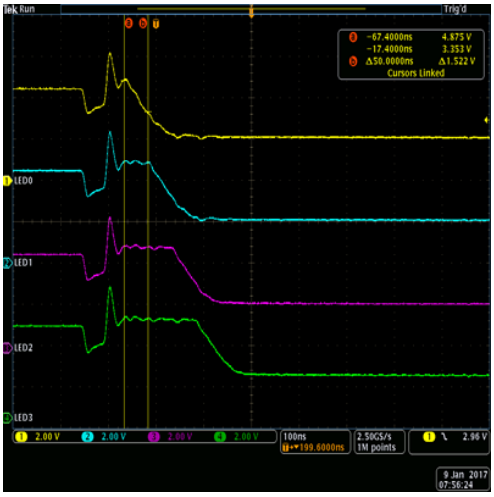

Figure 309. LED PWM Phase Shift 1

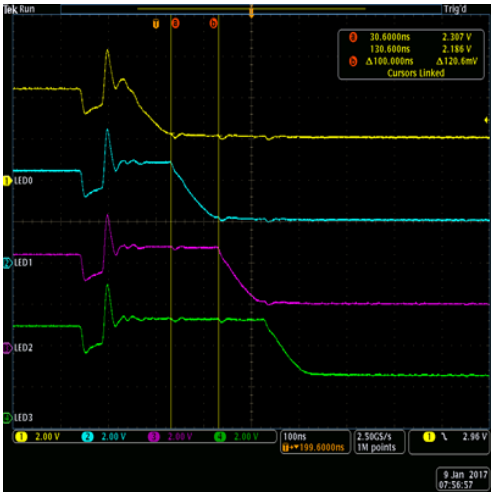

Figure 310. LED PWM Phase Shift 2

Figure 311. LED PWM Phase Shift 3

9 Power Supply Recommendations

9.1 Power Start-up and Shutdown Sequence

The preferred power start-up sequence for the LED171596A is to apply VDD first then VDDIO followed by VLED while keeping EN input low where t1 ≥ t2 ≥ 0 (refer to Figure 20). The VDD and VDDIO supplies can be applied simultaneously provided that VDD ≥ VDDIO in transition. The preferred power shutdown sequence is the exact opposite of start-up, EN set low then VLED removed followed by VDDIO removed and finally VDD removed where t1 ≥ t2 ≥ t3 ≥ 0 (refer to Figure 21).

9.2 VLED Input Supply Recommendations

The LED171596A is designed to operate from a 0-V to 6.1-V VLED voltage supply. The VLED supply must be well regulated and able to provide the peak current required by the LED configuration without voltage drop under load transients (start-up or rapid brightness change). The resistance of the input supply rail must be low enough such that the input current transient does not cause the VLED supply voltage to droop below LED V_f + VSAT voltage. TI recommends bulk decoupling located close to the VLED pin to minimize the impact of the VLED input supply rail resistance.

9.3 VDD Input Supply Recommendations

The LED171596A is designed to operate from a 2.9-V to 3.5-V VDD voltage supply. This input supply must be well regulated and be able to provide the peak current required by the LED configuration. The resistance of the VDD supply rail must be low enough such that the input current transient does not cause the LED171596A VIN supply voltage to droop below the maximum VDD_{POR} voltage. Additional bulk decoupling located close to the VDD bypass capacitor may be required to minimize the impact of the VDD input supply rail resistance.

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10 Layout

10.1 Layout Guidelines

See Figure 312 for the recommended layout of the LED171596A, which is designed for common system ground connections. Therefore, connect GND and LGND pins to the exposed thermal pad and the system ground. The GND plane connections to CVLED and GND pins must be on TOP layer copper with multiple vias connecting to system ground plane keeping traces as short as wide as possible.

Provide low inductive and resistive paths for loops with high di/dt. Therefore, paths conducting the switched load current (VLED, HS3, HS2, HS1 and HS0) must be as short and wide as possible. Parallel wiring over long distances, as well as narrow traces, must be avoided. Loops that conduct an alternating current must outline an area as small as possible, as this area is proportional to the energy radiated.

The exposed thermal pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation.

10.2 Layout Example

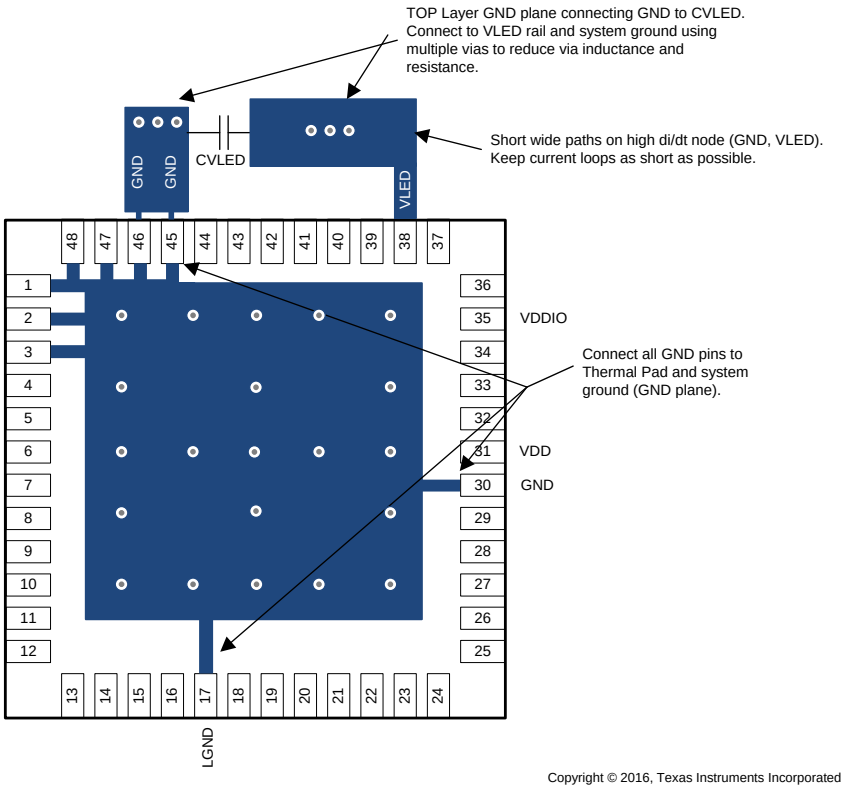

Figure 312. Layout Example

10.3 Thermal Information

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the exposed thermal pad
- Introducing airflow in the system

For more details on how to use the thermal parameters, see *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* and *Semiconductor and IC Package Thermal Metrics*.

The LED171596A is designed for a maximum operating junction temperature (T_J) of 125°C. Therefore, the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. Because the thermal resistance of the package is fixed, increasing the size of the surrounding copper area and improving the thermal connection to the device can reduce the thermal resistance. To get an improved thermal behavior, TI recommends using top-layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the device for improved thermal performance.

If short circuit or overload conditions are present, the device is protected by limiting internal power dissipation.

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Related Documentation

For additional information, see the following:

- *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*
- *Semiconductor and IC Package Thermal Metrics*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

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11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LED171596ARSLR	ACTIVE	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	L171596A A2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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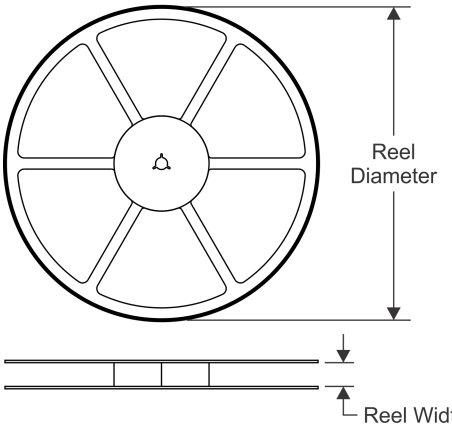
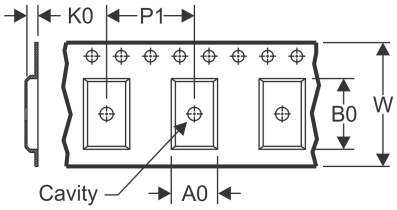
TAPE AND REEL INFORMATION

REEL DIMENSIONS

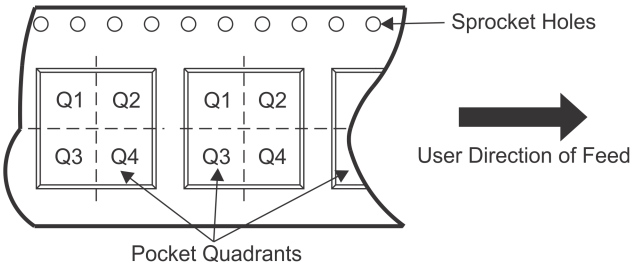


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

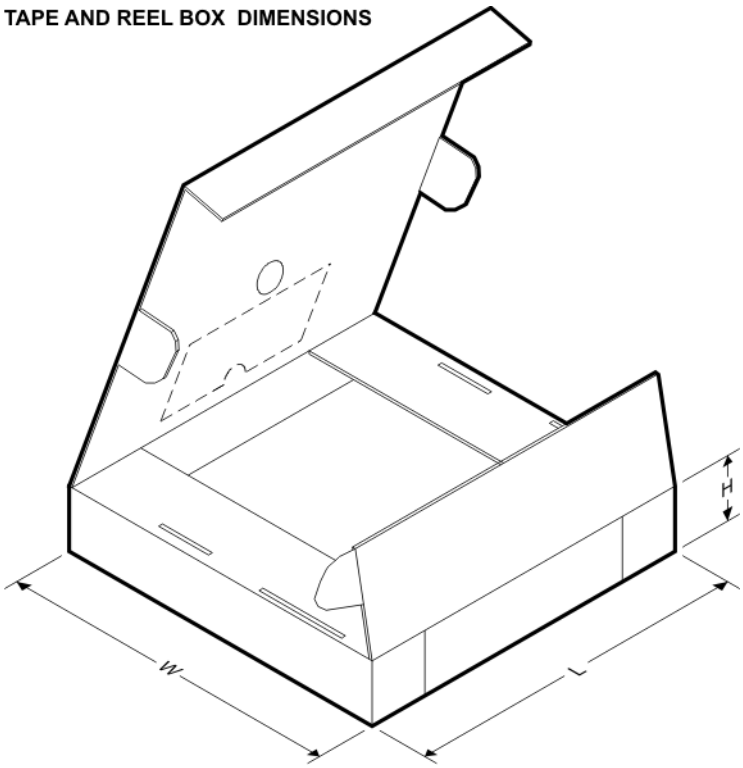
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LED171596ARSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

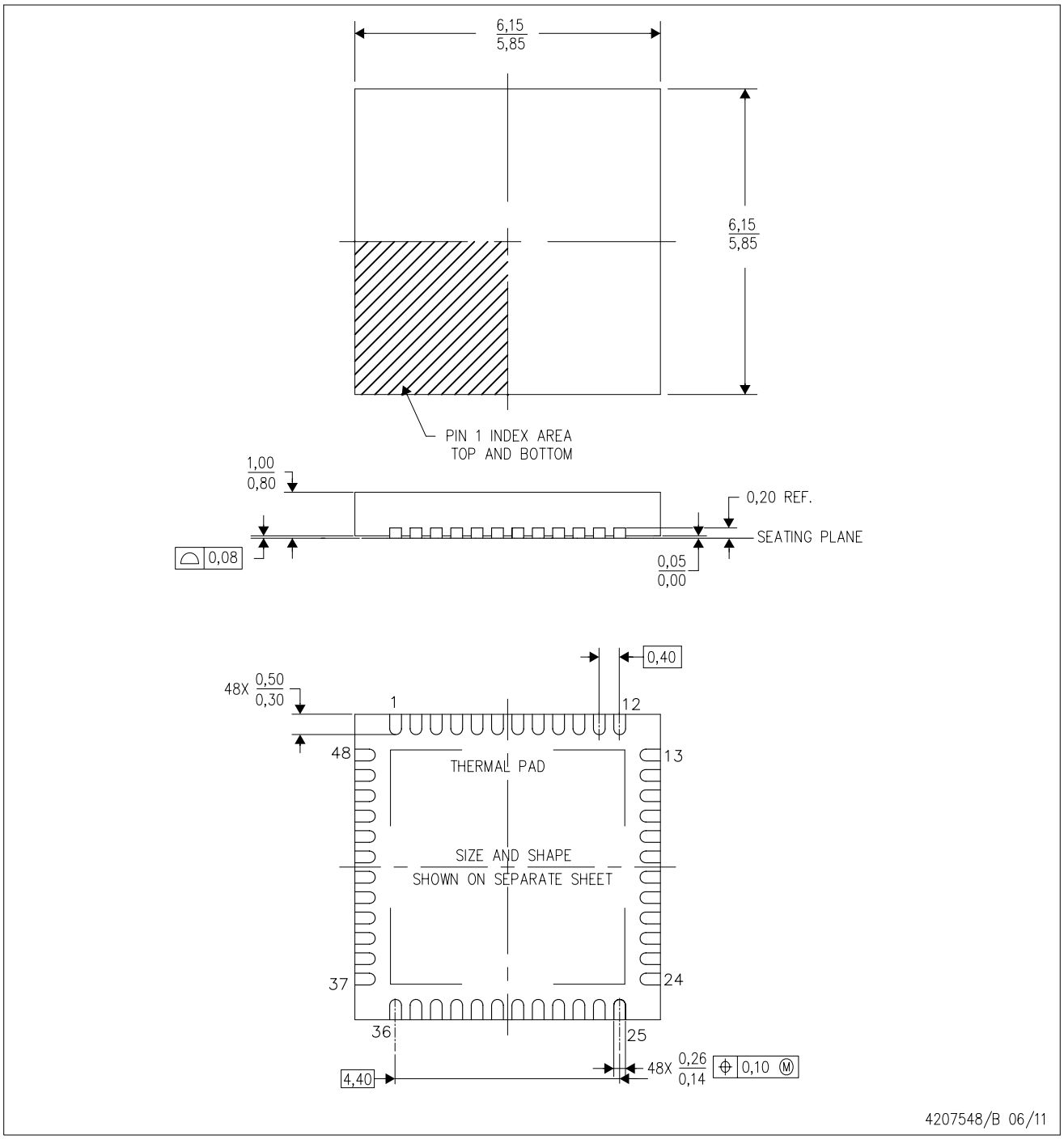
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LED171596ARSLR	VQFN	RSL	48	2500	367.0	367.0	35.0

RSL (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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